CAT. NO. 91

data delay devices, inc. ®

THE SOURCE

Active

Passive

Programmable

DDU-39

DMT-300

2214

PDU-13256

1517

MDU-4

1500

PDU-1364

DDU-4

1509

DDU-7J

1505

PPG-36

DDU-8

1503

1507

PDU-713

SMD-99

1503J

1519

PDU-138
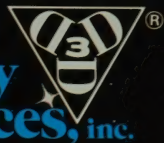
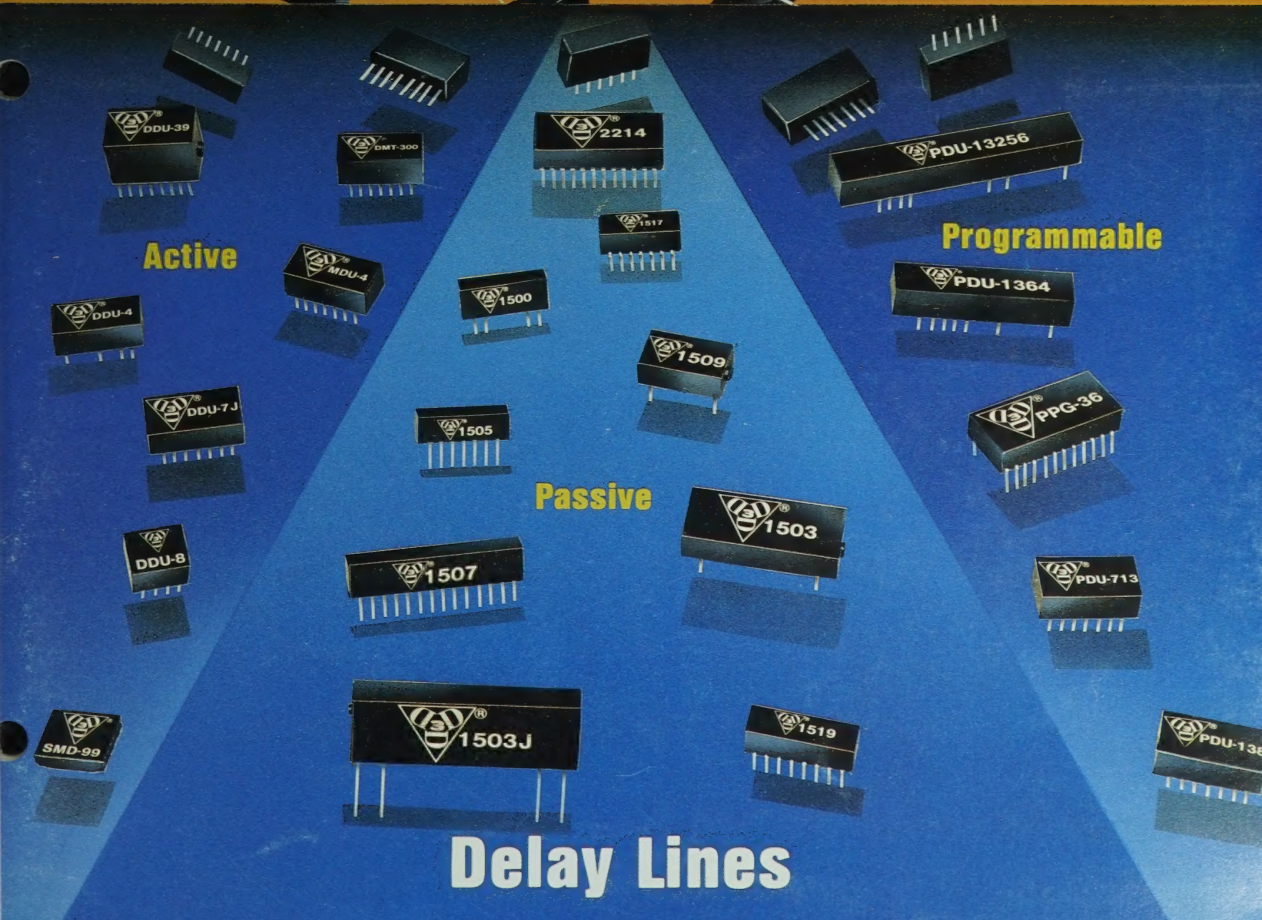# Delay Lines

data delay devices, inc.

COMPANY PROFILE

DATA DELAY DEVICES, INC. was founded in 1964 with the goal of becoming a major supplier of delay line components to the electronic industry with emphasis on quality, reliability and service. Today we supply products to more than 5,000 accounts. They include all the computer companies, the telecommunication companies, and the military and aerospace industry.

DATA DELAY DEVICES, INC. is a designer, developer and manufacturer of analog and digital delay lines, delay line application modules and filters. Our products range from the simplest delay lines of fixed delay, tapped delay, trimmer delay to the most sophisticated delay lines of digitally programmable delay lines, digitally programmable pulse generators, dynamic memory timers, gated oscillators and pulse controllers.

Our digital delay lines are completely interfaced with the most commonly available semiconductor families such as TTL, FAST, ECL, 100K ECL, CMOS.

Our product mix is approximately 65% commercial and 35% military. Our customized business is approximately 30% of our total sales and it is a very vital component of our business.

DATA DELAY DEVICES, INC. has modern production facilities capable of producing 50,000 to 100,000 units per week. Additional facilities are available to improve production rates if needed. We have the latest test equipment available in the industry and we have an automated computerized system that quickly tests and records data on the finished products prior to shipment.

We pride ourselves in our quality control department. Personnel is well qualified and dedicated to keeping our high quality standard in our products. Our quality control system is in accordance with MIL-1-45208, our sampling plan is in accordance with MIL-STD 105 and our calibration system is in accordance with MIL-STD-45662A. Every shipment to our customers is certified to meet appropriate specifications (i.e. either our standard published catalogs, specification data sheets or customer generated control documents).

We take pride in servicing our accounts with timely and friendly response to their needs. Let us be your reliable and quality supplier of delay lines. Call us.

N. Lupi, Pres.

GENERAL INFORMATION

ORDER INFORMATION:

Terms of Sale:
Net 30 Days if credit is established.
C.O.D. if credit is not established.
F.O.B. Point: Clifton, New Jersey

Orders may be placed direct by calling our Clifton, N.J. office or through any of the regional offices listed on last page.

APPLICATION ASSISTANCE

If you would like assistance in a new application, in preparing specifications, in testing, or in any other area, we welcome the opportunity to help you. Call us in Clifton, N.J. and ask for an Application Engineer, or call any of our Regional Offices.

DATA AND PRICES SUBJECT TO CHANGE WITHOUT NOTICE.

WARRANTY

1. DATA DELAY DEVICES, INC. warrants to the original purchaser that all products shall be free from defects in material or workmanship at time of shipment. Our obligation under this warranty is limited to the repairing or replacing of any of our products, providing said products are used within the specified ratings and applied in accordance with good engineering practice, and providing said products are proved by our examination to be defective and are returned to us transportation charges prepaid. This warranty shall constitute the fulfillment of the company's liability, and the company shall not be liable for any consequential damage. This warranty does not extend to any of our products which have been subject to misuse, neglect, accident, improper application or installation, nor shall it extend to material which has been altered or repaired outside our factory. This warranty is in lieu of all other warranties expressed or implied.

2. CLAIMS-DEFECTIVE MERCHANDISE:

   A. Damage in transit;
      File claim with carrier.
      Title also passes at F.O.B. point.

   B. Examination of merchandise:
      Any claim for shortage, defects or errors in shipment, must be made in writing within 15 days after receipt of goods.

   C. Returned Material:
      Units must be returned in the same or similar shipping containers. Return of parts will not be accepted unless previously authorized by the company through the issuance of a Return Material Authorization Number (RMA NO.) This RMA No. must be clearly displayed on the container's outside label.

data delay devices, inc. ®

Table of Contents

List By Function

List By Function (continued)

			LOGIC FAMILY					
		Page	TTL S	TTL FAST	ECL 10K	ECL 10KH	ECL 100K	H-CMOS
Active Programmable Delay Lines								
PDU-10256H series	8-Bit Programmable, 48 pins DIP	.52				●		
PDU-13256 series	8-Bit Programmable, 48 pins DIP	.53	●					
Active Programmable Pulsers								
Timing definition for PPG-33F to PPG-38F		.54						
PPG-33F series	3-Bit Programmable, 14 pins DIP	.55		●				
PPG-36F series	6-Bit Programmable, 24 pins DIP	.56		●				
PPG-38F series	8-Bit Programmable, 40 pins DIP	.57		●				
PPG-312F series	12-Bit Programmable, 40 pins DIP	.58		●				
VPG-40 series	Variable Pulse Generator	.59		●				
Active Pulse-Width Controllers								
PWC-11 series	Pulse Width Controller, 16 pins DIP	.60				●		
PWC-30 series	Pulse-Width Controller; 14 pins DIP	.61		●				
PWC-32 series	2-Pulse-Width Controllers, 14 pins DIP	.62		●				
Active Programmable Pulse Discriminators								
PPD-23 series	3-Bit Programmable	.63	●					
PPD-56 series	6-Bit Programmable	.64, 65		●				
Active Delay Line Oscillators								
DLO-31F series	Gated; 14 pins DIP, 2-⊖	.66		●				
DLO-32F series	Gated; 14 pins DIP, 2-⊖	.67		●				
PDO-1600 series	Gated; 16-Bit Programmable	.68		●				
Active Dynamic Memory Timers								
DMT-300 series	DRAM Timer, 14 pins DIP	.69	●					
Active Manchester Coders								
MAD-85 series	Decoder; 14 pins DIP	.70		●				
MAE-86 series	Encoder; 14 pins DIP	.71	●					
MAE-8782 series	Encoder; 20 MBAUD, 24 pins DIP	.72, 73		●				
MAD-8783 series	Decoder; 20 MBAUD, 24 pins DIP	.74, 75		●				
MAR-90 series	Repeater; 24 pins DIP	.76		●				
Active Filters								
5151 series	Low-Pass, 16 pins DIP	.77						
5353 series	High-Pass, 16 pins DIP	.77						
Passive Delay Lines								
1502 series	Fixed, 14 pins DIP	.78						
1503 & 1503J series	Continuously Variable, Trim-Dip	.79						
1504 series	Fixed, 16 pins DIP	.80						
1505 series	5 Taps, 7 Pins SIP	.81						
1507 series	10 Taps, 14 pins SIP	.82						
1509 & 1509J series	Continuously Variable, Mini-Trim	.83						
1513 series	Fixed, High Frequency, 4 pins SIP	.84						
1514 series	Fixed, High Frequency, 4 pins SIP	.85						
1517 series	5 Taps, 14 pins DIP	.86						
1519 series	10 Taps, 16 pins DIP	.87						
2020 series	Fixed, PICO seconds, 6 pins SIP	.88						
2211 series	Fixed, 24 pins DIP	.89						
2214 series	20 Taps, 24 pins DIP	.90						
Case Outlines		.91, 92, 93						

Specs & prices subject to change without notice.

Test Set-Up And Wave Forms

Passive Delay Line

TEST SET-UP

WAVEFORM
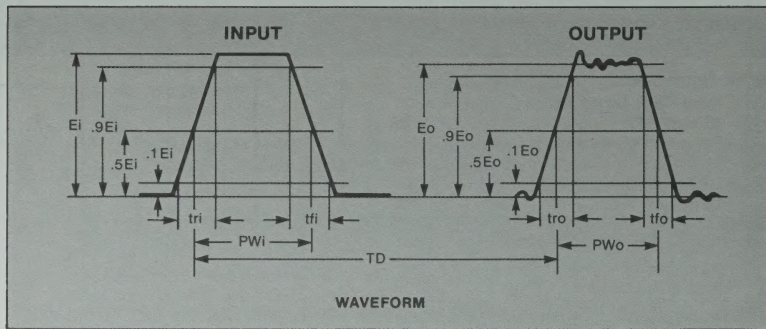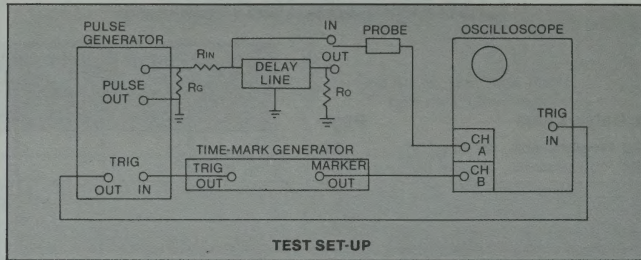
Active Delay Line (H-CMOS)

TEST SET-UP

WAVEFORM
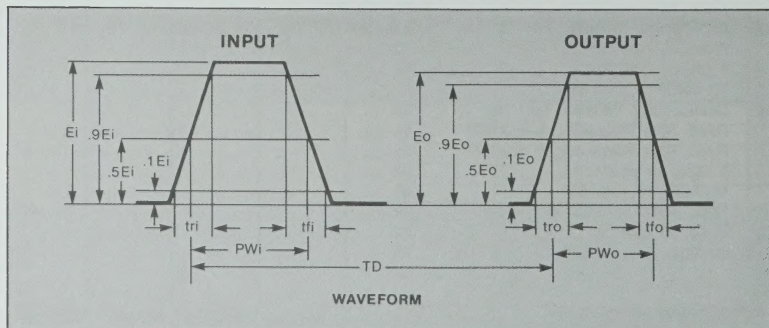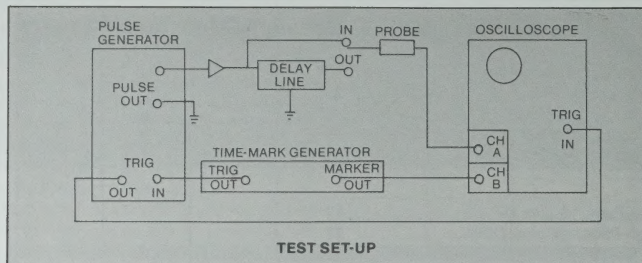
Active Delay Line (TTL)

TEST SET-UP

WAVEFORM
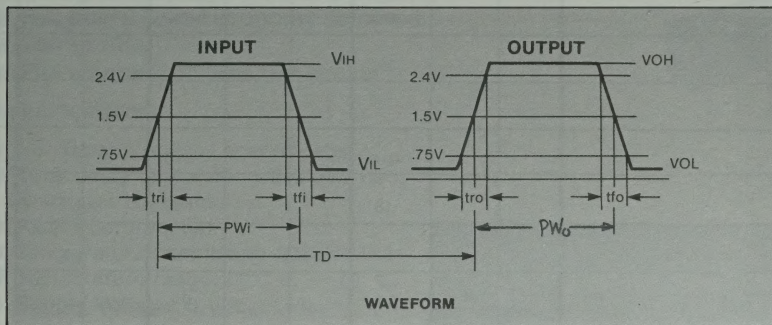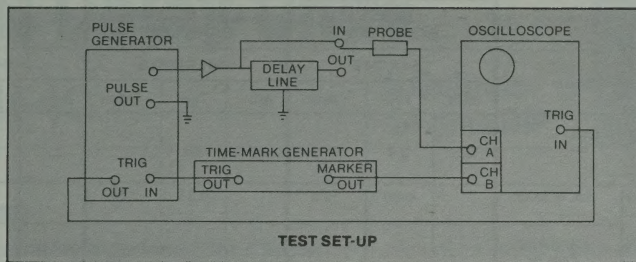
Active Delay Line (ECL)

TEST SET-UP

WAVEFORM
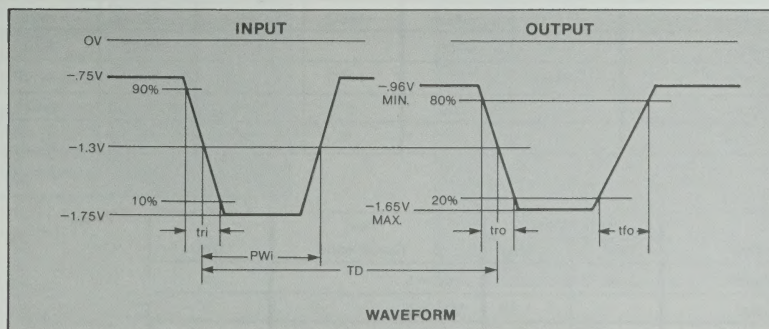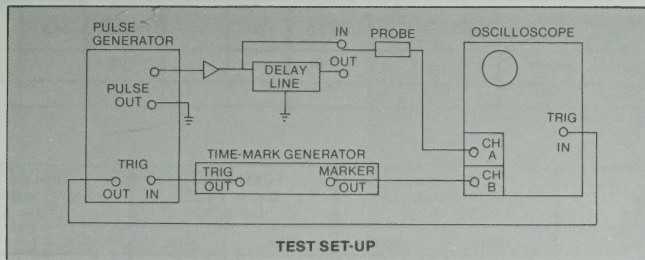
Ei	: Input pulse voltage	tri	: Input pulse rise time	VOL	: Low level output voltage
Eo	: Output pulse voltage	tfi	: Input pulse fall time	VOH	: High level output voltage
TD	: Delay time	tro	: Output pulse rise time	VIL	: Low level input voltage
PWi	: Input pulse width	tfo	: Output pulse fall time	VIH	: High level output voltage
PWo	: Output pulse width				

DC Electrical Characteristics

TTL – LOGIC

Parameter	Test Conditions[1]	FAST SCHOTTKY 54F/74F			LOW POWER SCHOTTKY 54LS/74LS			STANDARD SCHOTTKY 54S/74S			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	2.5	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN I_{OL} = MAX		0.35	0.5		0.35	0.5			0.5	V
	I_{OL} = 4mA (74LS)					0.25	0.4				V
I_{OH} HIGH-level output current				-1000			-400			-1000	μA
I_{OL} LOW-level output current				20			8			20	mA
V_{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL} LOW-level input voltage				+0.8			+0.8			+0.8	V
I_{IK} Input clamp current				-18			-18			-18	mA
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-1.2			-1.5			-1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX V_I = 7.0V			0.1			0.1			1.0	mA
I_{IH} HIGH-level input current	V_{CC} = MAX V_I = 2.7V			20			20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX V_I = 0.5V			-.6			-.4			-2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX	-60		-150	-20		-100	-40		-100	mA
OUTPUT FAN-OUT	HIGH			25			20			20	Unit Load
	LOW			12.5			10			10	

ECL – LOGIC

Symbol	Parameter	10K Series -30°C to 85°C V_{EE} -5.2V		10KH Series 0°C to 75°C V_{EE} -5.2V		100K Series 0°C to 85°C V_{EE} -4.5V		Unit
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	-1060	-700	-1020	-735	-1025	-880	mV
V_{OL}	Output LOW voltage	-1890	-1615	-1950	-1600	-1810	-1620	mV
V_{IH}	Input HIGH voltage		-700		-1070	-1165	-880	mV
V_{IL}	Input LOW voltage	-1890		-1480		-1810	-1475	mV
I_{IH}	Input HIGH current		350		475		340	μA
I_{IL}	Input LOW current	.5		.5		.5		μA

HCMOS – LOGIC

Symbol	Parameter	54HC/74HC		Test Conditions	Unit
		Min	Max		
V_{IH}	Input HIGH voltage	3.15		V_{CC} = 5	V
V_{IL}	Input LOW voltage		1.35	V_{CC} = 5	V
V_{OH}	Output HIGH voltage	3.98		V_{CC} = 5; -I_o = 4 ma	V
V_{OL}	Output LOW voltage		.26	V_{CC} = 5; I_o = 4 ma	V
$\pm I_I$	Input leakage current		.10	V_{CC} = 5	μA
$\pm I_{OZ}$	3-state OFF-state current		.5	V_{CC} = 5	μA

HCMOS–Logic
Digital Delay Units
SERIES: DDU-4C

5 Outputs
14 pins DIP

data
delay
devices, inc. ®

Features:

■ Completely interfaced for CMOS.
■ No external components required.
■ P.C. board space economy achieved.
■ Low profile.
■ Fits standard 14 pins DIP socket.

Specifications:

■ **No. Taps:** 5 equally spaced taps.
■ **Total delay tolerance:** ±5% or 2 ns whichever is greater.
■ **Rise time:** 8 ns typ.
■ **Temperature coefficient:** 300 PPM/°C.
■ **Temperature range:** 0° C to + 70° C.
■ **Supply Voltage:** 5 Vdc ± 5%.
■ **Supply current:**
  I_{CCH} = 10 ma
  I_{CCL} = 40 μa
■ **Fan-out:** 10 LSTTL loads min.
■ **DC Parameters:** See HCMOS-Logic Table on Page 6.
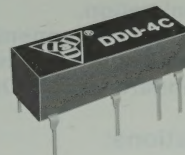
Part No.	Total Delay (ns)	Tap Delay (ns)
DDU-4C-5050	50	10 ± 2
DDU-4C-5060	60	12 ± 2
DDU-4C-5075	75	15 ± 2
DDU-4C-5100	100	20 ± 2
DDU-4C-5125	125	25 ± 2
DDU-4C-5150	150	30 ± 3
DDU-4C-5175	175	35 ± 3
DDU-4C-5200	200	40 ± 4
DDU-4C-5250	250	50 ± 5

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.780 MAX.
.290 MAX.
.015 TYP.
.018 TYP.
.070 MAX.
.600 ± .010
.280 MAX.
.010 ± .002
.350 MAX.

Tap #	1	2	3	4	5
Pin #	12	4	10	6	8

Vcc 14
IN 1
G 7
R
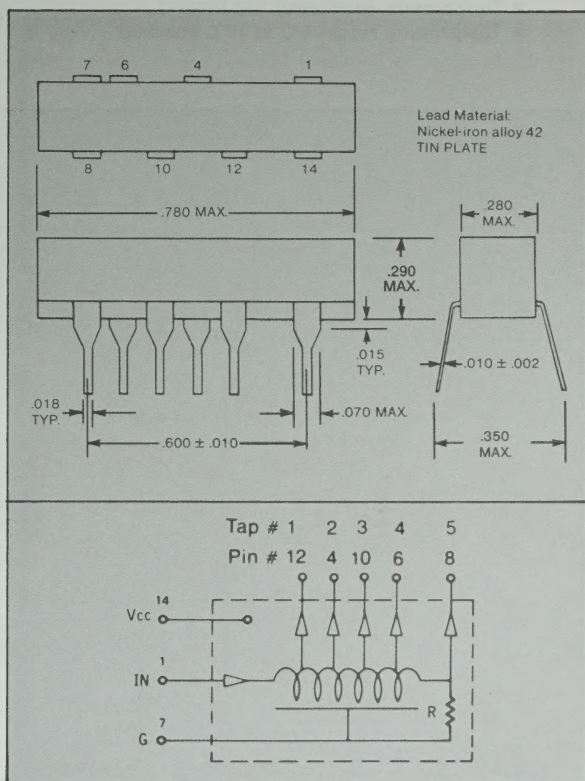
Fast Logic

Digital Delay Units
SERIES: DDU-4F 1 to 5 Taps (14 pins DIP) TTL Interfaced

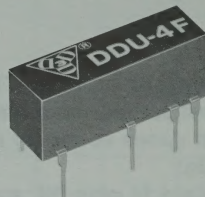**data delay devices, inc.**

Features:

- Auto-insertable.
- Completely interfaced with TTL and DTL application.
- No external components required.
- P.C. board space economy achieved.
- Fits standard 14 pins DIP socket.

Specifications:

- Delay tolerance: ±5% or better or 2 ns whichever is greater.
- Rise-time: 2 ns typically.
- Temperature coefficient: 100 PPM/°C.
- Temperature range: 0°C to 70°C standard.

- Minimum pulse width: 20% of total delay.
- Supply voltage: 4.75 to 5.25 Vdc.
- Supply current:
  I_{CCL}: 32 ma.
  I_{CCH}: 7 ma.

- DC Parameters: See TTL-Fast Schottky Logic Table on Page 6.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.780 MAX.
.280 MAX.
.290 MAX.
.015 TYP.
.010 ± .002
.018 TYP.
.070 MAX.
.600 ± .010
.350 MAX.

Tap #	1	2	3	4	5
Pin #	12	4	10	6	8

14 Vcc
1 IN
7 G
R
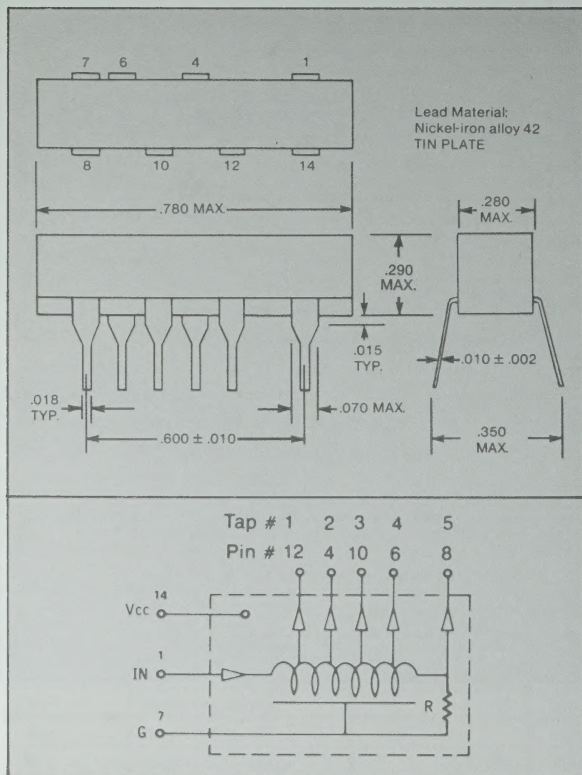
Single Delay Output (ns)		2 Delays Output (ns)		
Part No.	Delay @ Pin #8	Part No.	Delay @ Pin #10	Delay @ Pin #8
DDU-4F-1010	10	DDU-4F-2020	10	20
DDU-4F-1020	20	DDU-4F-2040	20	40
DDU-4F-1030	30	DDU-4F-2050	25	50
DDU-4F-1040	40	DDU-4F-2060	30	60
DDU-4F-1050	50	DDU-4F-2080	40	80
DDU-4F-1060	60	DDU-4F-2100	50	100
DDU-4F-1080	80	DDU-4F-2150	75	150
DDU-4F-1100	100	DDU-4F-2200	100	200
DDU-4F-1150	150	DDU-4F-2300	150	300
DDU-4F-1200	200	DDU-4F-2400	200	400
DDU-4F-1300	300	DDU-4F-2500	250	500
DDU-4F-1400	400	DDU-4F-7690A	65	110
DDU-4F-1500	500			

5 Delays Output (ns)				
Part No.	Delay @ Pin #12	Delay @ Pin #4	Delay @ Pin #10	Delay @ Pin #6	Delay @ Pin #8
DDU-4F-5025	5	10	15	20	25
DDU-4F-5050	10	20	30	40	50
DDU-4F-5075	15	30	45	60	75
DDU-4F-5100	20	40	60	80	100
DDU-4F-5125	25	50	75	100	125
DDU-4F-5150	30	60	90	120	150
DDU-4F-5200	40	80	120	160	200
DDU-4F-5250	50	100	150	200	250
DDU-4F-5300	60	120	180	240	300
DDU-4F-5400	80	160	240	320	400
DDU-4F-5500	100	200	300	400	500

Digital Delay Units

SERIES: DDU-5J

10 Taps (32 pins DIP)
T²L Interfaced

data delay devices, inc. ®
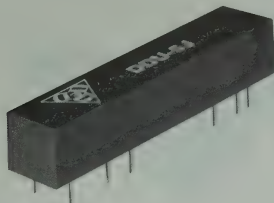
Features:

- Completely interfaced for TTL and DTL applications.
- No external components required.
- 10 Taps equally spaced.
- P. C. board space economy achieved.

Specifications:

- **Delay tolerance:** ±5% or better, or 2 ns whichever is greater.
- **Rise-time:** 4 ns typically.
- **Temperature coefficient:** 100 PPM/°C.
- **Temperature range:** −0°C to 70°C standard. (−55°C. to +125°C. on request)*
- **Supply voltage:** 5 Vdc ± 5%.
- **Power dissipation:** 780 mw max.
- **DC Parameters:** See TTL-Standard Schottky Logic Table on Page 6.

*Add "M" after Part No. Example DDU-5J-1010M
**.320 Max. for "M" Units

Part No.	Total Delay (ns)	Delay Per Tap (ns)
DDU-5J-10050	50	5
DDU-5J-10100	100	10
DDU-5J-10150	150	15
DDU-5J-10200	200	20
DDU-5J-10250	250	25
DDU-5J-10300	300	30
DDU-5J-10400	400	40
DDU-5J-10500	500	50
DDU-5J-101000	1000	100
DDU-5J-101500	1500	150
DDU-5J-102000	2000	200

† or case stand-offs

TAP #	1	2	3	4	5	6	7	8	9	10
PIN #	30	4	28	6	26	21	13	19	15	17
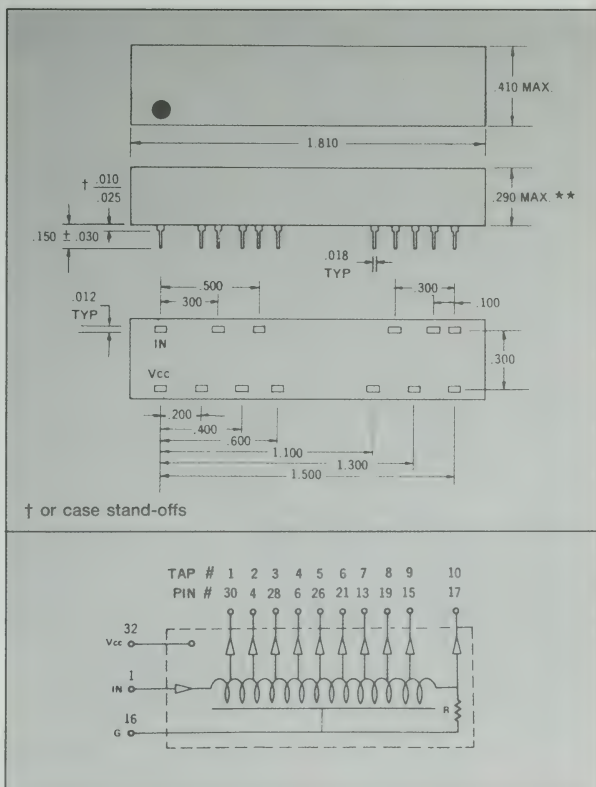
HCMOS — Logic

Digital Delay Units

SERIES: DDU-7C

10 Outputs
16 pins DIP

data
delay
devices, inc.
®

Features:

- Completely interfaced for HCMOS application
- No external components required
- P.C. board space economy achieved
- Fits standard 16 pins DIP socket
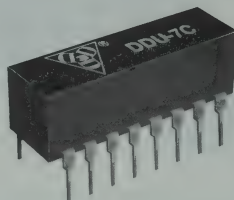- Operates over commercial temperature range

Specifications:

- **No. Taps:** 10 equally spaced taps.
- **Total delay tolerance:** ±5% or 2 ns whichever is greater.
- **Rise time:** 8 ns typ.
- **Temperature coefficient:** 300 PPM/°C.
- **Temperature range:** 0° C to + 70° C.
- **Supply Voltage:** 5 Vdc ± 5%.
- **Supply current:**
  I_{CCH} = 10 ma
  I_{CCL} = 40 μa
- **Fan-out:** 10 LSTTL loads min.
- **DC Parameters:** See TTL-HCMOS Logic Table on Page 6.
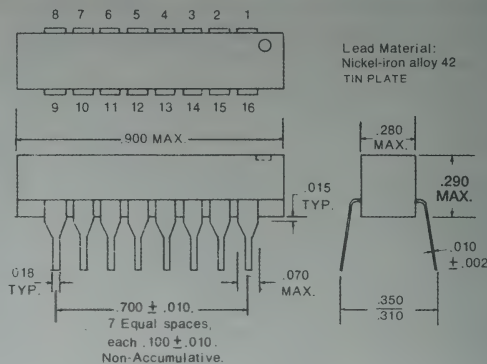
Part No.	Total Delay (ns)	Delay Per Tap (ns)
DDU-7C-100	100	10.0 ± 2
DDU-7C-150	150	15.0 ± 2
DDU-7C-200	200	20.0 ± 2
DDU-7C-250	250	25.0 ± 2
DDU-7C-300	300	30.0 ± 3
DDU-7C-400	400	40.0 ± 4
DDU-7C-500	500	50.0 ± 5

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.900 MAX.
.280 MAX.
.290 MAX.
.015 TYP.
.010 ± .002
.018 TYP.
.070 MAX.
.350 / .310
.700 ± .010.
7 Equal spaces,
each .100 ± .010.
Non-Accumulative.

Tap #	1	2	3	4	5	6	7	8	9	10
Pin #	15	2	14	3	13	4	12	5	11	6

V CC
16 In
1
GRD
8
R

Digital Delay Units

SERIES: DDU-7F

10 Taps (14 pins DIP)
TTL Interfaced

data delay devices, inc. ®

Features:

- Auto-insertable.
- Completely interfaced for TTL
- No external components required
- P.C. board space economy achieved
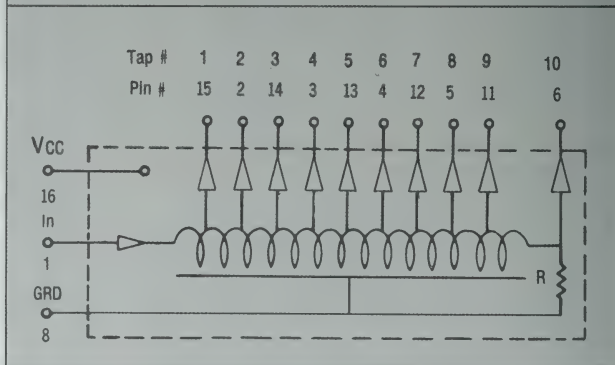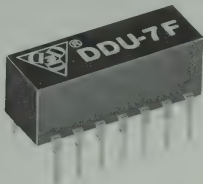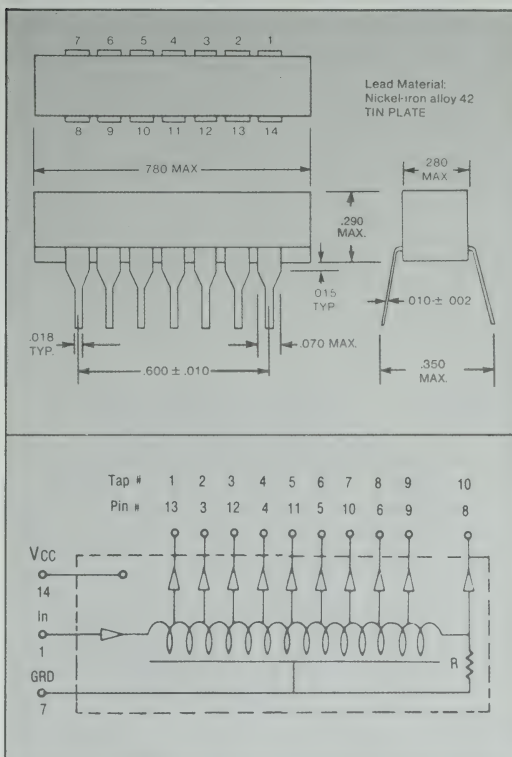- Fits standard 14 pins DIP socket

Specifications:

- **No. Taps:** 10 equally spaced.
- **Total Delay Tolerance:** ±5% or better, or 2 ns whichever is greater.
- **Rise time:** 2 ns typically.
- **Temperature coefficient:** 100 PPM/°C.
- **Temperature range:** 0° to + 70°C. (−55°C to +125°C on request.)*
- **Supply voltage:** 4.75 to 5.25 V.
- **Supply Current:**
  I$_{CCL}$: 50 ma.
  I$_{CCH}$: 15 ma.
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.

*Add "M" to Part No.: Ex. DDU-7F-100ME5.
 Case size: E5.

Part No.	Total Delay (ns)	Delay Per Tap (ns)
*DDU-7F-10	9	1 ÷ .4
*DDU-7F-20	18	2 ÷ .5
*DDU-7F-25	22.5	2.5 ÷ .7
DDU-7F-50	50	5.0 ÷ 1.5
DDU-7F-100	100	10.0 ÷ 2
DDU-7F-150	150	15.0 ÷ 2
DDU-7F-200	200	20.0 ÷ 2
DDU-7F-250	250	25.0 ÷ 2
DDU-7F-300	300	30.0 ÷ 3
DDU-7F-400	400	40.0 ÷ 4
DDU-7F-500	500	50.0 ÷ 5

*Time delay referenced to 1st tap.
 3.5 ns ± 1 ns inherent delay.

Test Conditions:

- Input Pulse Width: ≥150% of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Unless otherwise specified all time-delays are referenced to input of delay line.
- Rise-time is measured from .75 V to 2.4 V of leading edge.
- All measurements made @ V$_{cc}$ = 5V; T$_A$ = +25°C.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

780 MAX
280 MAX
.290 MAX.
.015 TYP.
.010 ± .002
.018 TYP.
.070 MAX.
.350 MAX.
.600 ± .010

Tap #	1	2	3	4	5	6	7	8	9	10
Pin #	13	3	12	4	11	5	10	6	9	8

V$_{CC}$ 14
In 1
GRD 7
R

HCMOS–Logic
Digital Delay Units

SERIES: DDU-8C

**5 Outputs
8 pin DIP**

**data
delay
devices, inc.** ®

Features:

■ **Low Cost.**
■ **Completely interaced for CMOS.**
■ **Low profile.**
■ **Fits standard 8 pins DIP socket.**

Specifications:

■ **No. Taps:** 5 equally spaced taps.
■ **Total delay tolerance:** ±5% or 2 ns
whichever is greater.
■ **Rise time:** 8 ns typ.
■ **Temperature coefficient:** 300 PPM/°C.
■ **Temperature range:** 0° C to + 70° C.
■ **Supply Voltage:** 5 Vdc ± 5%.
■ **Supply current:**
  I_{CCH} = 10 ma
  I_{CCL} = 40 µa
■ **Fan-out:** 10 LSTTL loads min.
■ **DC Parameters:** See HCMOS-Logic Table on
Page 6.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.500
.280 MAX.
.290 MAX.
.015 TYP.
.010 ± .002
.018 TYP.
.070 MAX.
.300
.350 MAX.

Part No.	Total Delay (ns)	Tap Delay (ns)
DDU-8C-5050	50	10 ± 3
DDU-8C-5060	60	12 ± 3
DDU-8C-5075	75	15 ± 3
DDU-8C-5100	100	20 ± 3
DDU-8C-5125	125	25 ± 3
DDU-8C-5150	150	30 ± 3
DDU-8C-5175	175	35 ± 4
DDU-8C-5200	200	40 ± 4
DDU-8C-5250	250	50 ± 5

Tap # 1 2 3 4 5
Pin # 7 2 6 3 5

Vcc 8
IN 1
G 4

Digital Delay Units

SERIES: DDU-8F

**TTL Interfaced,5 Outputs
8 pin DIP**

**data
delay
devices, inc.**
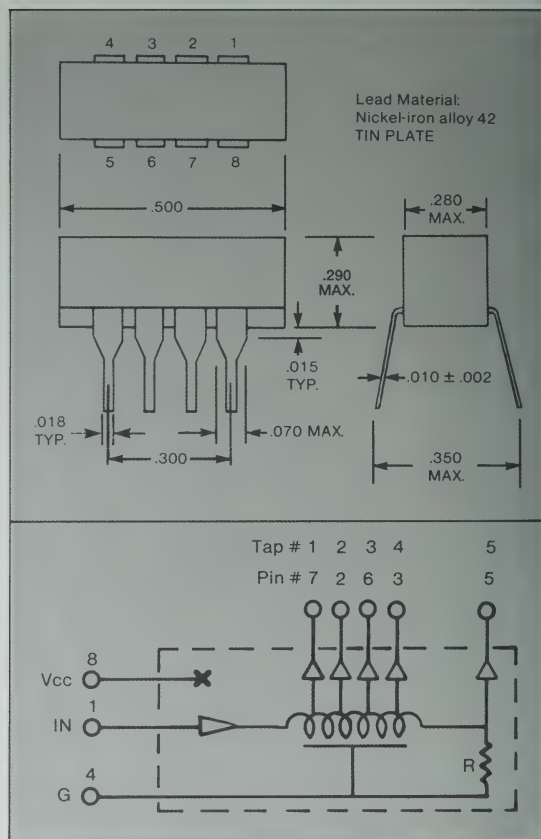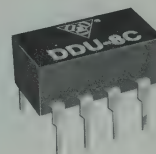
Features:

- Auto-insertable.
- Low Cost.
- Completely interfaced for TTL.
- Low profile.
- Fits standard 8 pins DIP socket.

Specifications:

- **Outputs:** 5, equally spaced.
- **Delay tolerance:** see table.
- **Rise-time:** 2 ns typ.
- **Minimum pulse width:** 40% of total delay.
- **Temperature range:** 0° C to + 70° C.
- **Temperatue coefficient:** 100 PPM/°C.
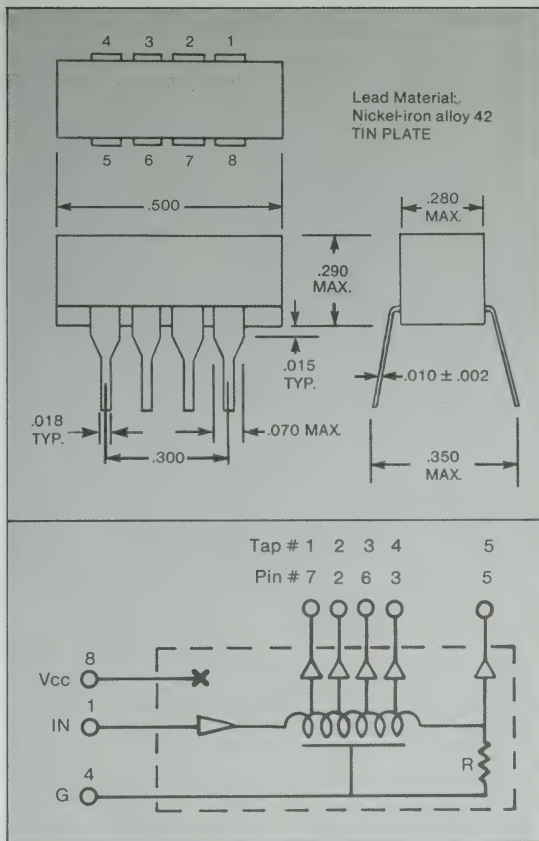- **Supply voltage:** 4.75 to 5.25 Vdc.
- **Supply current:**
  - **Iccl:** 32 ma.
  - **Icch:** 7 ma.
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Part No.	Total Delay (ns)	Tap Delay (ns)
*DDU-8F-5004	4 ± 1	1 ± 0.5
*DDU-8F-5006	6 ± 1	1.5 ± 0.5
*DDU-8F-5008	8 ± 2	2 ± 1
*DDU-8F-5010	10 ± 2	2.5 ± 1
*DDU-8F-5012	12 ± 2	3 ± 1
*DDU-8F-5016	16 ± 2	4 ± 1.5
*DDU-8F-5020	20 ± 3	5 ± 2
DDU-8F-5030	30 ± 3	6 ± 2
DDU-8F-5035	35 ± 3	7 ± 2
DDU-8F-5040	40 ± 3	8 ± 2
DDU-8F-5045	45 ± 3	9 ± 3
DDU-8F-5050	50 ± 3	10 ± 3
DDU-8F-5060	60 ± 3	12 ± 3
DDU-8F-5075	75 ± 4	15 ± 3
DDU-8F-5100	100 ± 5	20 ± 3
DDU-8F-5125	125 ± 6.5	25 ± 3
DDU-8F-5150	150 ± 7.5	30 ± 3
DDU-8F-5175	175 ± 8	35 ± 4
DDU-8F-5200	200 ± 10	40 ± 4
DDU-8F-5250	250 ± 12.5	50 ± 5

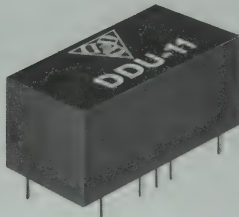*Time delay measured with respect to 1st tap.
3.5 ns ± 1 ns inherent delay.

Lead Material:.
Nickel-iron alloy 42
TIN PLATE

.500

.280 MAX.

.290 MAX.

.015 TYP.

.010 ± .002

.018 TYP.

.070 MAX.

.300

.350 MAX.

Tap # 1 2 3 4 5

Pin # 7 2 6 3 5

8 Vcc

1 IN

4 G

R

Digital Delay Units

SERIES DDU-11   5 Taps ECL Interfaced

data delay devices, inc. ®

Test Conditions:

- Input pulse-width: 150% of total delay.
- Input pulse rise-time: ≤6 ns.
- Input pulse voltage: −.7V
- Rise-time measured from 20% to 80% of leading edge.
- Delay time measured at 50% of leading edge.
- All measurements taken @ V_{EE} = −5.2V and T_A = 25°C.
- Unless otherwise specified, all time-delays are referenced to the input pin.

Features:

- **Input & Output Buffered**
- **5 Equally Spaced Taps**
- **Fits in Standard 16 Pins DIP**
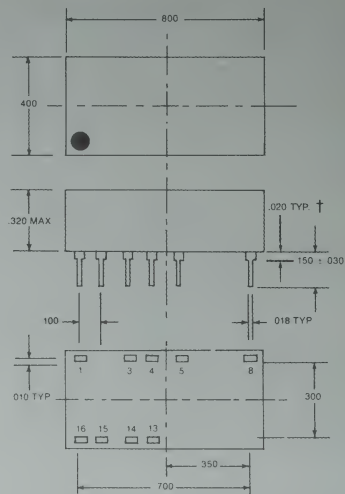
Specifications:

- **Total Delay Tolerance:** ± 5% or better, or 2 ns whichever is greater.
- **No. Taps:** 5 equally spaced.
- **Rise-time:** 2 ns typical.
- **Supply voltage:** −5.2V
- **Operating Temperature:** −30°C to 85°C.
- **Power Dissipation:** −200 mw typ. (no load).
- **Temperature coefficient:** 100 PPM/°C.
- **DC Parameters:** See ECL-10K Logic Table on Page 6.

Part No.	Total Delay (ns)	Delay Tap (ns)
*DDU-11-5	4	1 ± .3
*DDU-11-10	8	2 ± .4
*DDU-11-20	16	4 ± .5
*DDU-11-25	20	5 ±1.0
DDU-11-50	50	10 ±2.0
DDU-11-75	75	15 ±2.0
DDU-11-100	100	20 ±2.0
DDU-11-150	150	30 ±2.0
DDU-11-200	200	40 ±2.0
DDU-11-250	250	50 ±2.5
DDU-11-300	300	60 ±3.0
DDU-11-400	400	80 ±4.0
DDU-11-500	500	100 ±5.0

*Time delay measurements referenced to 1st tap.
3.5 ns ± 1 ns inherent delay.

† or case stand-offs

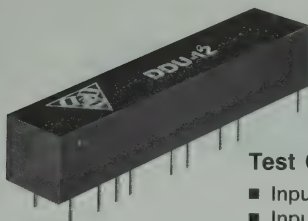Tap # 1 2 3 4 5
Pin # 15 3 14 4 13
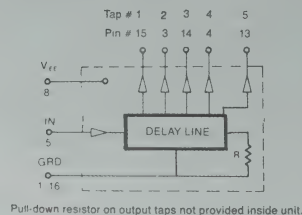
Pull-down resistor on output taps not provided inside unit.

14

Digital Delay Units

SERIES DDU-12   10 Taps ECL Interfaced

data delay devices, inc. ®

Features:

- **Input & Output ECL Buffered**
- **10 Equally Spaced Taps**
- **PC Board Economy Achieved**
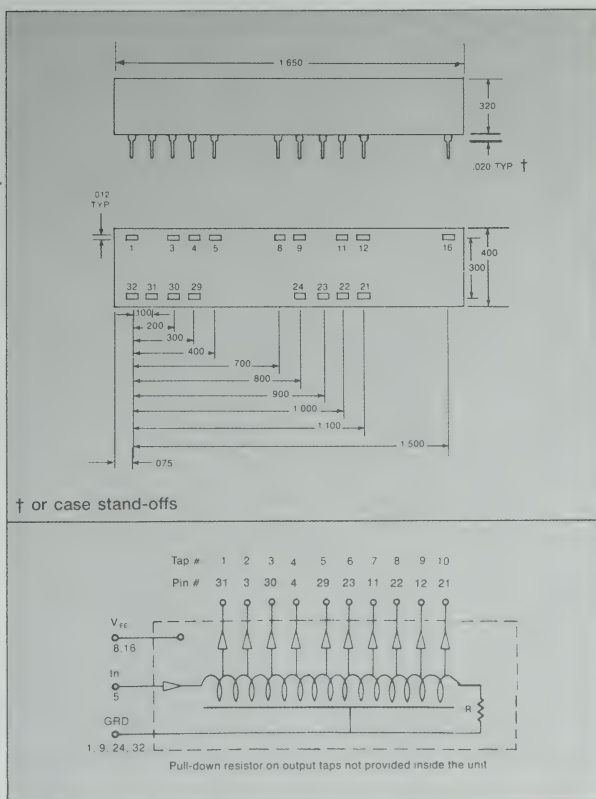
Specifications:

- **Total Delay Tolerance:** ± 5% or better, or 2 ns whichever is greater.
- **No. Taps:** 10 equally spaced.
- **Rise-time:** 2 ns typical.
- **Supply voltage:** −5.2V
- **Operating Temperature:** −30°C to 85°C.
- **Power Dissipation:** −400 mw typ. (no load).
- **Temperature coefficient:** 100 PPM/°C.
- **DC Parameters:** See ECL-10K Logic Table on Page 6.

Test Conditions:

- Input pulse-width: 150% of total delay.
- Input pulse rise-time: ≤6 ns.
- Input pulse voltage: −.7V
- Rise-time measured from 20% to 80% of leading edge.
- Delay time measured at 50% of leading edge.
- All measurements taken @ V_{EE} = −5.2V and T_A = 25°C.
- Unless otherwise specified, all time-delays are referenced to the input pin.

Part No.	Total Delay (ns)	Tap Delay (ns)
*DDU-12-10	9	1 ± .3
*DDU-12-20	18	2 ± .4
*DDU-12-25	22.5	2.5 ± .4
*DDU-12-40	36	4 ± .5
*DDU-12-50	45	5 ± 1.0
DDU-12-75	75	7.5 ± 1.5
DDU-12-100	100	10 ± 2.0
DDU-12-150	150	15 ± 2.0
DDU-12-200	200	20 ± 2.0
DDU-12-250	250	25 ± 2.0
DDU-12-300	300	30 ± 2.0
DDU-12-400	400	40 ± 2.0
DDU-12-500	500	50 ± 2.5
DDU-12-750	750	75 ± 4.1
DDU-12-1000	1000	100 ± 5.0
DDU-12-1500	1500	150 ± 7.0

*Time delay measurements referenced to 1st tap.
 3.5 ns ± 1 ns inherent delay.

† or case stand-offs

Pull-down resistor on output taps not provided inside the unit

100K ECL Digital Delay Unit

SERIES: DDU-18
100K ECL Interfaced
24 Pin DIP

data delay devices, inc.
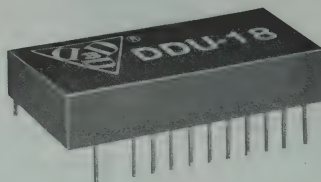
Features:

- Input & output buffered.
- 8 equally spaced taps.
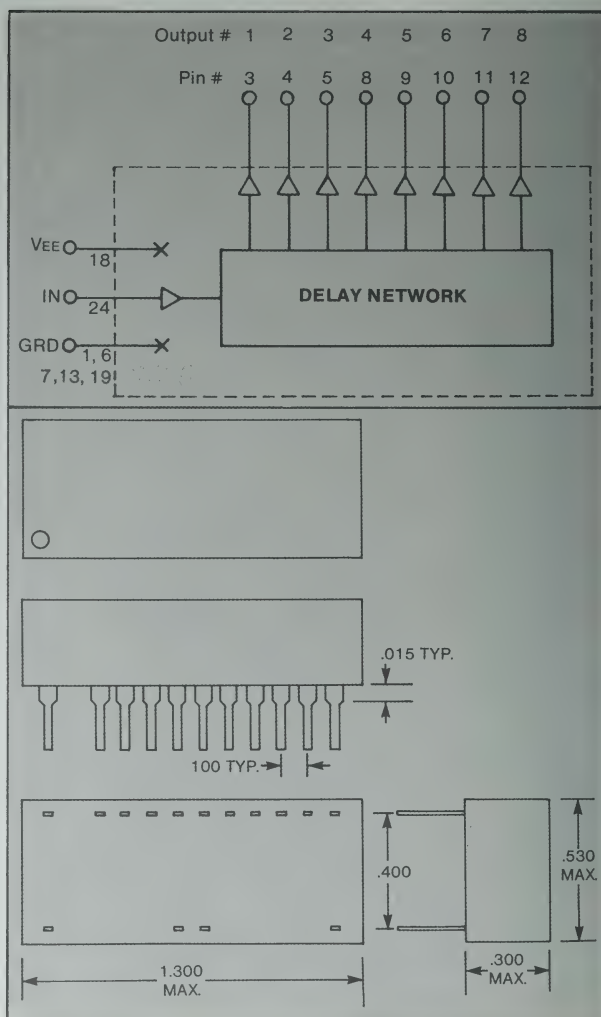- Compatible with ECL circuits.

Specifications:

- **Total delay tolerance:** ±5% or 1 ns whichever is greater.
- **No. taps:** 8 equally spaced.
- **Rise time:** 1 ns typ.
- **Input pulse width:** 40% of total delay.
- **Input PRR:** 3 × PW.
- **Input pulse voltage:** .8V p-p (−.9V to −1.7V).
- **Supply Voltage (Vee):** −4.5V.
- **Supply current (Vee):** 100 ma typ.
- **Operating temperature:** 0°C to +85°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Fan-out capabilities:** 70 ECL.
- **DC Parameters:** See ECL-100K Logic Table on Page 6.

Part No.	Delay Increment (ns)	Total Delay (ns)
*DDU-18-4	.5	3.5
*DDU-18-8	1	7.0
*DDU-18-12	1.5	10.50
DDU-18-16	2	16
DDU-18-20	2.5	20
DDU-18-24	3	24
DDU-18-32	4	32
DDU-18-40	5	40
DDU-18-48	6	48
DDU-18-56	7	56
DDU-18-64	8	64
DDU-18-72	9	72
DDU-18-80	10	80
DDU-18-100	12.5	100
DDU-18-120	15	120
DDU-18-160	20	160
DDU-18-200	25	200

We customize.
*Referenced to 1st tap. 2 ns ± 1 ns inherent delay.

Output #	1	2	3	4	5	6	7	8
Pin #	3	4	5	8	9	10	11	12

VEE O 18
IN O 24
GRD O 1, 6, 7, 13, 19

DELAY NETWORK

.015 TYP.
100 TYP.
.400
.530 MAX.
1.300 MAX.
.300 MAX.

Fast Logic
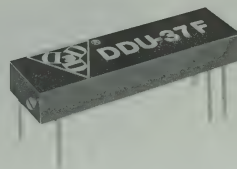# Digital Delay Unit

SERIES: DDU-37F

Continuously Variable T²L Interfaced

data delay devices, inc. ®

Features:

- Input & output fully TTL Interfaced & buffered.
- Low profile.
- Commercial & military type.
- Continuously adjustable.
- Multi-turn adjusting screw (40 turns approx.)

Specifications:

- **Inherent delay (T_{DO}):** 6 ns typ.
- **Delay resolution:** .12 ns.
- **Output rise-time:** 4 ns typ.
- **Temperature coefficient:** 100 PPM/°C.
- **Temperature range:** 0°C to 70°C standard. (−55°C to +125°C on request)*
- **Supply voltage:** 5.0 Vdc ±5%.
- **Power Dissipation:** 230 mw max.
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.

* Add "M" after Part No. Ex.: DDU-37F-50M.
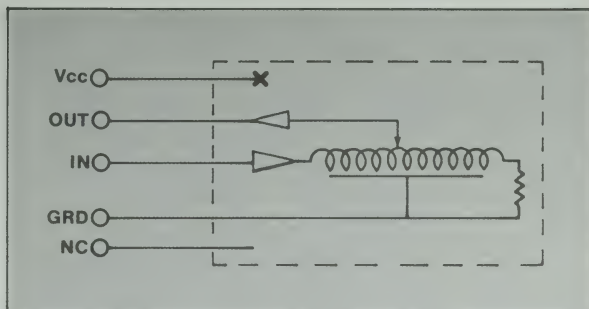
Part No.	Min. Delay Variation (ns)
DDU-37F-25	15
DDU-37F-30	20
DDU-37F-40	30
DDU-37F-50	40
DDU-37F-60	50
DDU-37F-70	60
DDU-37F-80	70
DDU-37F-100	90
DDU-37F-120	100
DDU-37F-150	130
DDU-37F-200	180

Other delay times available on request.
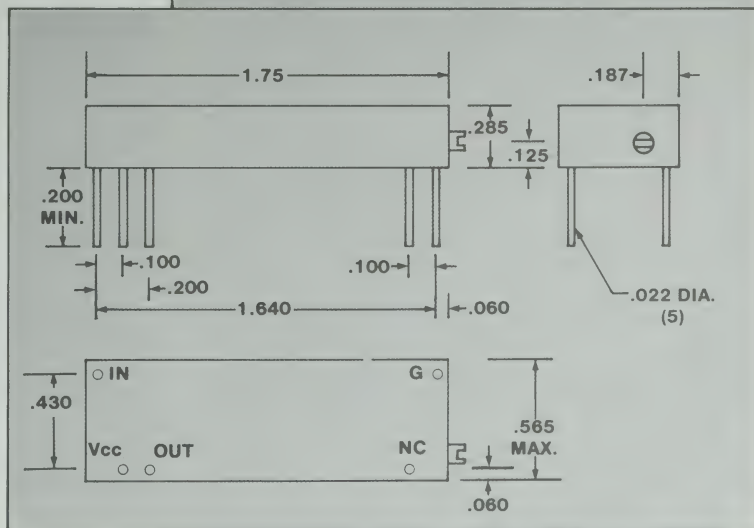
Digital Delay Units

SERIES: DDU-39F

Continuously Variable TTL Interfaced

data delay devices, inc.

Features:

- Completely interfaced with TTL.
- 0.5 ns adjustment resolution.
- Fits standard 16 pin DIP sockets.

Specifications:

- **Temperature coefficient:** 220 PPM/°C.
- **Rise-Time:** 4 ns typically.
- **Temperature range:** 0° C to 70° C standard.
  (−55° C to +125° C on request)*
- **Supply voltage:** 5 Vdc ±5%.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

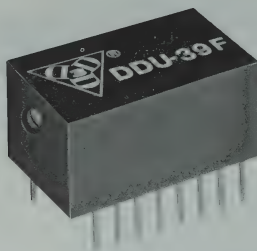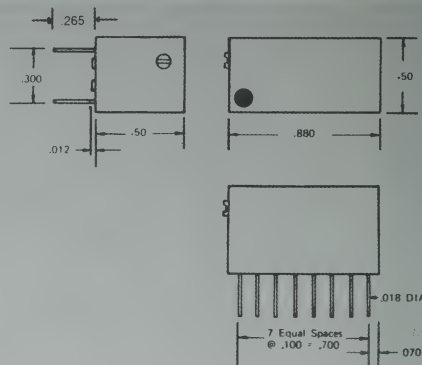| Part No.	Inherent Delay Typ.	Adjustment Range Typ.	Power Dissipation
DDU-39F	7 ns	7 ns to 25 ns	230 mw Max.
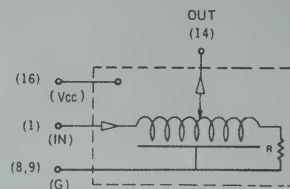
Fast Logic
Digital Delay Units
SERIES: DDU-47F

**Continuously Variable
TTL Interfaced**

data delay devices, inc. ®
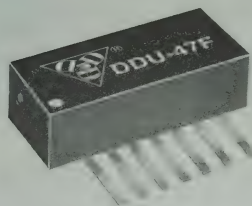
Features:

- **Completely interfaced with TTL.**
- **.25 ns adjustment resolution.**
- **Surface mount.**

Specifications:

- **Temperature coefficient:** 220 PPM/°C.
- **Rise-Time:** 2 ns typically.
- **Temperature range:** 0° C to 70° C standard.
  (−55° C to +125° C on request)*
- **Supply voltage:** 5 Vdc ± 5%.
- **DC parameters:** See TTL-Fast Schottky Logic Table on
  Page 6.

Part No.	Inherent Delay Typ.	Adjustment Range Typ.	Power Dissipation
DDU-47F	5 ns	5 ns to 25 ns	230 mw Max.
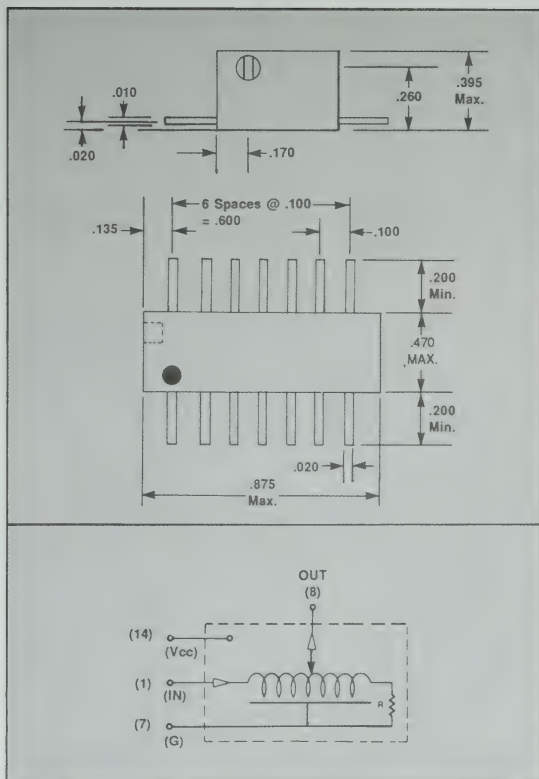
HCMOS — Logic
Digital Delay Units
SERIES: DDU-66C

5 Outputs
14 pin DIP

data delay devices, inc. ®
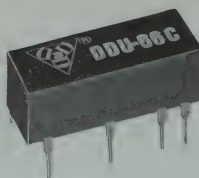
Features:
- Automatic insertable.
- Low Cost.

Specifications:

- **No. Taps:** 5 equally spaced taps.
- **Total delay tolerance:** ±5% or 2 ns whichever is greater.
- **Rise time:** 8 ns typ.
- **Temperature coefficient:** 300 PPM/°C.
- **Temperature range:** 0° C to + 70° C.
- **Supply Voltage:** 5 Vdc ± 5%.
- **Supply current:**
  I_{CCH} = 10 ma
  I_{CCL} = 40 μa
- **Fan-out:** 10 LSTTL loads min.
- **DC parameters:** See HCMOS-Logic Table on Page 6.

Part No. Table

DDU-66C (Standard)	Total Delay (ns)	Tap Delay (ns)
DDU-66C-50	50 ± 3	10 ± 3
DDU-66C-60	60 ± 3	12 ± 3
DDU-66C-75	75 ± 4	15 ± 3
DDU-66C-100	100 ± 5	20 ± 3
DDU-66C-125	125 ± 6.5	25 ± 3
DDU-66C-150	150 ± 7.5	30 ± 3
DDU-66C-175	175 ± 8	35 ± 4
DDU-66C-200	200 ± 10	40 ± 4
DDU-66C-250	250 ± 12.5	50 ± 5

Tap # 1 2 3 4 5
Pin # 12 4 10 6 8

14 Vcc
1 IN
7 G
R

7 6 4 1
8 10 12 14

.780 MAX.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.280 MAX.
.290 MAX.
.015 TYP.
.010 ± .002
.018 TYP.
.070 MAX.
.600 ± .010
.350 MAX.
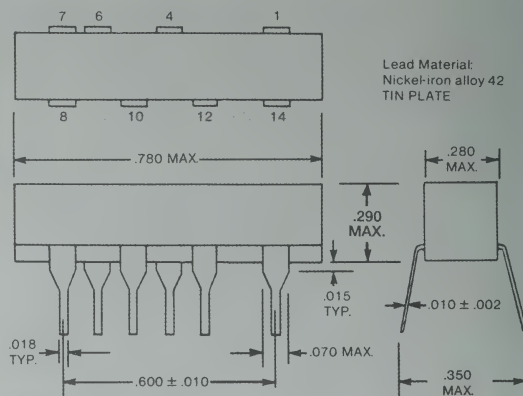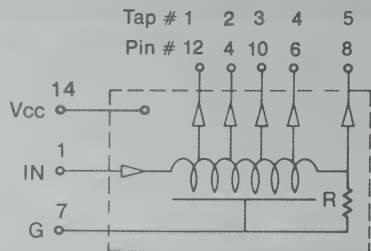
==== Fast Logic

Digital Delay Units

SERIES: DDU-66F

TTL Interfaced, 5 Outputs
14 pins DIP & Surface Mount

data delay devices, inc. ®

Features:

- Automatic insertable.
- Through-hole or surface mount leads.
- Low Cost.

Specifications:

- **Outputs:** 5, equally spaced.
- **Delay tolerance:** see table.
- **Rise-time:** 2 ns typically.
- **Minimum pulse width:** 40% of total delay.
- **Temperature range:** 0° C to + 70° C.
- **Temperatue coefficient:** 100 PPM/°C.
- **Supply voltage:** 4.75 to 5.25 Vdc.
- **Leads:** Alloy 42, tin plated.
- **Supply current:**
  - I_{CCL}: 32 ma.
  - I_{CCH}: 7 ma.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.
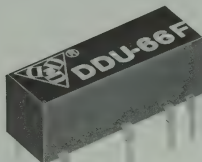
DDU-66F (Standard)	DDU-66F (Type "A")	DDU-66F (Type "B")	Total Delay (ns)	Tap Delay (ns)
*DDU-66F-4	*DDU-66F-4A	*DDU-66F-4B	4 ± 1	1 ± 0.5
*DDU-66F-6	*DDU-66F-6A	*DDU-66F-6B	6 ± 1	1.5 ± 0.5
*DDU-66F-8	*DDU-66F-8A	*DDU-66F-8B	8 ± 2	2 ± 1
*DDU-66F-10	*DDU-66F-10A	*DDU-66F-10B	10 ± 2	2.5 ± 1
*DDU-66F-12	*DDU-66F-12A	*DDU-66F-12B	12 ± 2	3 ± 1
*DDU-66F-16	*DDU-66F-16A	*DDU-66F-16B	16 ± 2	4 ± 1.5
*DDU-66F-20	*DDU-66F-20A	*DDU-66F-20B	20 ± 3	5 ± 2
DDU-66F-25	DDU-66F-25A	DDU-66F-25B	25 ± 3	5 ± 2
DDU-66F-30	DDU-66F-30A	DDU-66F-30B	30 ± 3	6 ± 2
DDU-66F-35	DDU-66F-35A	DDU-66F-35B	35 ± 3	7 ± 2
DDU-66F-40	DDU-66F-40A	DDU-66F-40B	40 ± 3	8 ± 2
DDU-66F-45	DDU-66F-45A	DDU-66F-45B	45 ± 3	9 ± 3
DDU-66F-50	DDU-66F-50A	DDU-66F-50B	50 ± 3	10 ± 3
DDU-66F-60	DDU-66F-60A	DDU-66F-60B	60 ± 3	12 ± 3
DDU-66F-75	DDU-66F-75A	DDU-66F-75B	75 ± 4	15 ± 3
DDU-66F-100	DDU-66F-100A	DDU-66F-100B	100 ± 5	20 ± 3
DDU-66F-125	DDU-66F-125A	DDU-66F-125B	125 ± 6.5	25 ± 3
DDU-66F-150	DDU-66F-150A	DDU-66F-150B	150 ± 7.5	30 ± 3
DDU-66F-175	DDU-66F-175A	DDU-66F-175B	175 ± 8	35 ± 3
DDU-66F-200	DDU-66F-200A	DDU-66F-200B	200 ± 10	40 ± 4
DDU-66F-250	DDU-66F-250A	DDU-66F-250B	250 ± 12.5	50 ± 5

*Time delay measured with respect to 1st tap. 3.5 ns ± 1 ns inherent delay.

Tap # 1 2 3 4 5
Pin # 12 4 10 6 8

14 Vcc
1 IN
7 G
R

STANDARD DIP-MOUNT

14 12 10 8
1 4 6 7
.780 MAX.
.275 ±.010
.290 MAX.
.015 TYP.
.010 ±.002
.150 MIN
.018 TYP.
.070 MAX.
.300 ±.005
.600±.010
6 Equal Spaces

TYPE "A" SURFACE MOUNT
.430
.070
.070
.010 TYP.

TYPE "B" SURFACE MOUNT
.310
.100
.100
.015 TYP.

HCMOS — Logic

Digital Delay Unit

SERIES: DDU-222C

5 Outputs
8 pins SIP

data delay devices, inc. ®

Features:

- ■ Very thin unit.
- ■ HCMOS input and outputs.
- ■ SIP package.
- ■ Economical.
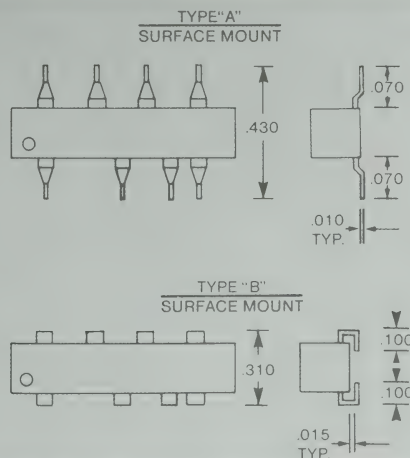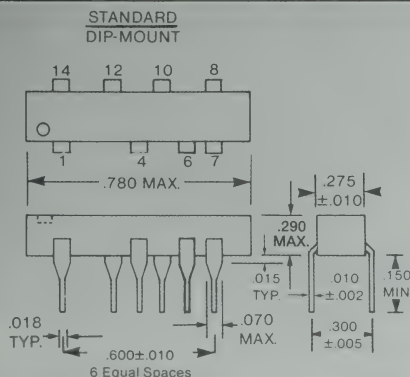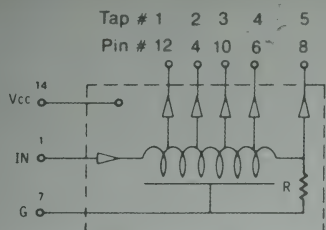
Specifications:

- ■ No. Taps: 5 equally spaced taps.
- ■ Total delay tolerance: ±5% or 2 ns whichever is greater.
- ■ Rise time: 8 ns typ.
- ■ Temperature coefficient: 300 PPM/°C.
- ■ Temperature range: 0°C to + 70°C.
- ■ Supply Voltage: 5 Vdc ± 5%.
- ■ Supply current:
  I_{CCH} = 10 ma
  I_{CCL} = 40 μa
- ■ Fan-out: 10 LSTTL loads min.
- ■ DC parameters: See HCMOS-Logic Table on Page 6.

Part No.	Total Delay (ns)	Tap Delay (ns)
DDU-222C-50	50 ± 3	10 ± 3
DDU-222C-60	60 ± 3	12 ± 3
DDU-222C-75	75 ± 4	15 ± 3
DDU-222C-100	100 ± 5	20 ± 3
DDU-222C-125	125 ± 6.5	25 ± 3
DDU-222C-150	150 ± 7.5	30 ± 3
DDU-222C-175	175 ± 8	35 ± 4
DDU-222C-200	200 ± 10	40 ± 4
DDU-222C-250	250 ± 12.5	50 ± 5

Fast Logic

Digital Delay Unit

SERIES: DDU-222F

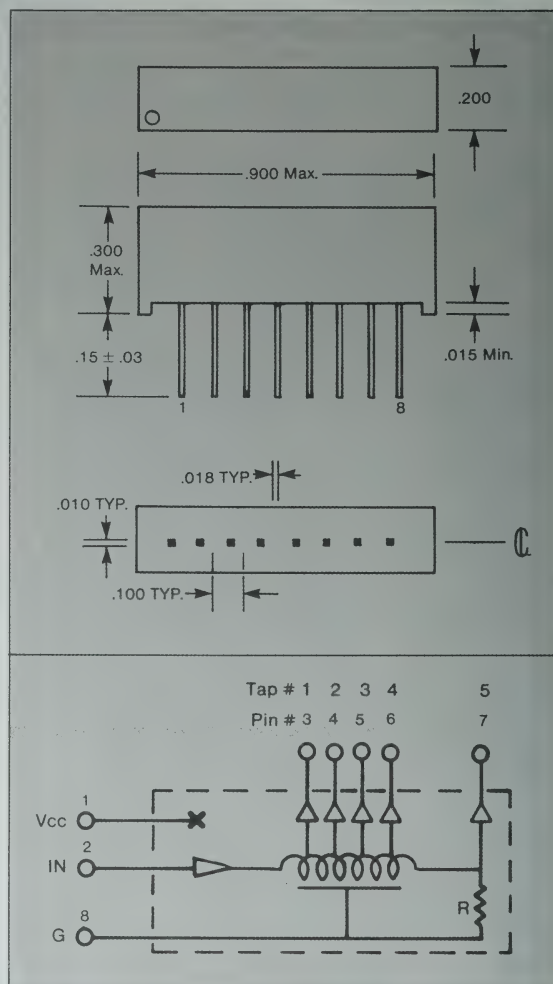**8 pins SIP**
T²L Interfaced

data delay devices, inc. ®

Features:

- Very thin unit.
- TTL input and outputs.
- SIP package.
- Economical.

Specifications:

- Outputs: 5, equally spaced.
- Delay tolerance: see table.
- Rise-time: 2 ns typ.
- Minimum pulse width: 40% of total delay.
- Temperature range: 0° C to + 70° C.
- Temperatue coefficient: 100 PPM/°C.
- Supply voltage: 4.75 to 5.25 Vdc.
- Supply current:
  - I_{CCL}: 32 ma.
  - I_{CCH}: 7 ma.
- DC parameters: See TTL-Fast Schottky Logic on Page 6.

Part No.	Total Delay (ns)	Tap Delay (ns)
*DDU-222F-4	4 ± 1	1 ± 0.5
*DDU-222F-6	6 ± 1	1.5 ± 0.5
*DDU-222F-8	8 ± 2	2 ± 1
*DDU-222F-10	10 ± 2	2.5 ± 1
*DDU-222F-12	12 ± 2	3 ± 1
*DDU-222F-16	16 ± 2	4 ± 1.5
*DDU-222F-20	20 ± 3	5 ± 2
DDU-222F-30	30 ± 3	6 ± 2
DDU-222F-35	35 ± 3	7 ± 2
DDU-222F-40	40 ± 3	8 ± 2
DDU-222F-45	45 ± 3	9 ± 3
DDU-222F-50	50 ± 3	10 ± 3
DDU-222F-60	60 ± 3	12 ± 3
DDU-222F-75	75 ± 4	15 ± 3
DDU-222F-100	100 ± 5	20 ± 3
DDU-222F-125	125 ± 6.5	25 ± 3
DDU-222F-150	150 ± 7.5	30 ± 3
DDU-222F-175	175 ± 8	35 ± 4
DDU-222F-200	200 ± 10	40 ± 4
DDU-222F-250	250 ± 12.5	50 ± 5

*Time delay measured with respect to 1st tap.
3.5 ns ± 1 ns inherent delay.

.200

.900 Max.

.300 Max.

.15 ± .03

.100 MIN.

1   8

.018 TYP.

.010 TYP.

.100 TYP.

Tap # 1 2 3 4   5
Pin # 3 4 5 6   7

1 Vcc

2 IN

8 G

R

Fast Logic
Digital Delay Units
SERIES: **DDU-224F** — 10 Taps (14 pins SIP) TTL Interfaced

data delay devices, inc. ®

Features:

- Completely interfaced for TTL
- No external components required
- P.C. board space economy achieved

Specifications:

- No. Taps: 10 equally spaced taps.
- Total Delay Tolerance: ±5% or better, or 2 ns whichever is greater
- Rise time: 2 ns typically.
- Temperature coefficient: 100 PPM/°C.
- Temperature range: 0° to + 70°C.
- Supply voltage: 4.75 to 5.25 V
- Supply Current:
  - I_{CCL}: 50 ma.
  - I_{CCH}: 15 ma.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.

Test Conditions:

- Input Pulse Width: ≥150% of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Unless otherwise specified all time-delays are referenced to input of delay line.
- Rise-time is measured from .75 V to 2.4 V of leading edge.
- All measurements made @ V_{cc}= 5V; T_A= +25°C.

Part Numbers	Tap Delay	Total Delay
*DDU-224F-10	1	9
*DDU-224F-20	2	18
*DDU-224F-25	2.5	22.5
*DDU-224F-50	5	45
DDU-224F-100	10	100
DDU-224F-150	15	150
DDU-224F-200	20	200
DDU-224F-250	25	250
DDU-224F-300	30	300
DDU-224F-400	40	400
DDU-224F-500	50	500

*Time delay referenced to tap #1.
3.5 ns ± 1 ns inherent delay.

Other delay times on request.
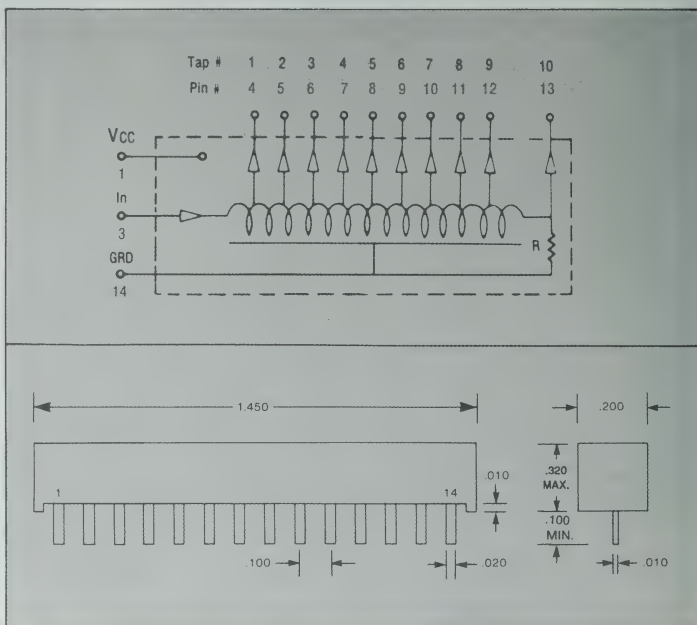
Fast Logic
Surface Mounted Delay Line

SERIES: SMD-91
TTL Interfaced

data delay devices, inc.

FEATURES:
- **Designed for surface mounting.**
- **Low profile .175 max. height.**
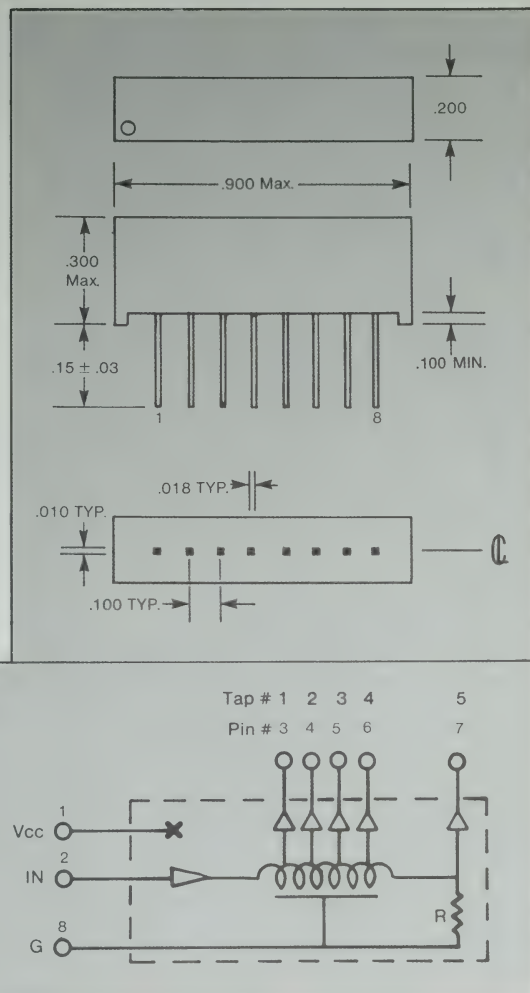- **Completely interfaced for TTL.**
- **Up to 5 outputs.**

Specifications:
- **Outputs:** 5, equally spaced.
- **Delay tolerance:** see table.
- **Rise-time:** 2 ns typically.
- **Minimum pulse width:** 40% of total delay.
- **Temperature range:** 0°C to 70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Supply voltage:** 4.75 to 5.25 Vdc.
- **Leads:** Alloy 42, tin plated.
- **Supply current:**
  - I_{CCL}: 32 ma.
  - I_{CCH}: 7 ma.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Part Number	Total Delay (ns)	Tap Delay (ns)
*SMD-91-5004	4 ± 1	1 ÷ 0.5
*SMD-91-5006	6 ± 1	1.5 ÷ 0.5
*SMD-91-5008	8 ± 2	2 ÷ 1
*SMD-91-5010	10 ± 2	2.5 ÷ 1
*SMD-91-5012	12 ± 2	3 ÷ 1
*SMD-91-5016	16 ± 2	4 ± 1.5
*SMD-91-5020	20 ÷ 3	5 ÷ 2
SMD-91-5030	30 ± 3	6 ± 2
SMD-91-5035	35 ± 3	7 ± 2
SMD-91-5040	40 ± 3	8 ± 2
SMD-91-5045	45 ± 3	9 ± 3
SMD-91-5050	50 ÷ 3	10 ÷ 3
SMD-91-5060	60 ± 3	12 ± 3
SMD-91-5075	75 ± 4	15 ± 3
SMD-91-5100	100 ÷ 5	20 ÷ 3
SMD-91-5125	125 ± 6.5	25 ± 3
SMD-91-5150	150 ± 7.5	30 ± 3
SMD-91-5175	175 ± 8	35 ± 4
SMD-91-5200	200 ± 10	40 ± 4
SMD-91-5250	250 ± 12.5	50 ± 5

*Time delay measured with respect to 1st tap.
3.5 ns ± 1 ns inherent delay.

HCMOS — Logic

Surface Mounted Delay Line

SERIES: **SMD-99C**
5 Outputs

data delay devices, inc. ®

Features:

■ Designed for surface mounting.
■ Low profile .175 max. height.
■ Completely interfaced HCMOS.

Specifications:

■ **No. Taps:** 5 equally spaced taps.
■ **Total delay tolerance:** ±5% or 2 ns whichever is greater.
■ **Rise time:** 8 ns typ.
■ **Temperature coefficient:** 300 PPM/°C.
■ **Temperature range:** 0°C to + 70°C.
■ **Supply Voltage:** 5 Vdc ± 5%.
■ **Supply current:**
  I_{CCH} = 10 ma
  I_{CCL} = 40 μa
■ **Fan-out:** 10 LSTTL loads min.
■ **DC parameters:** See HCMOS-Logic Table on Page 6.
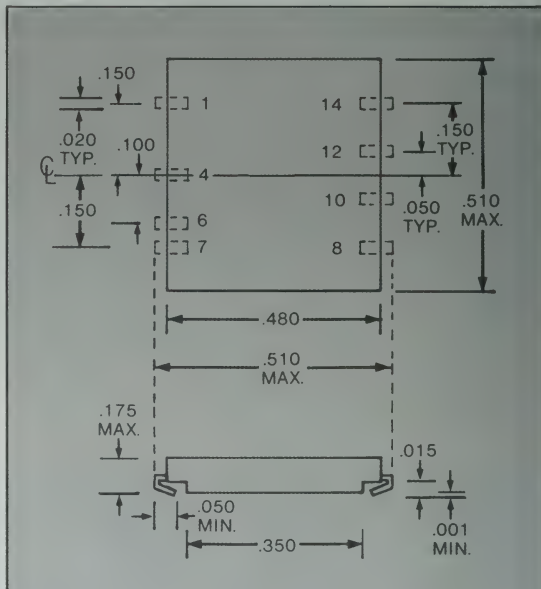
Part No.	Total Delay (ns)	Tap Delay (ns)
SMD-99C-5050	50± 3	10 ± 3
SMD-99C-5060	60 ± 3	12 ± 3
SMD-99C-5075	75 ± 4	15 ± 3
SMD-99C-5100	100 ± 5	20 ± 3
SMD-99C-5125	125 ± 6.5	25 ± 3
SMD-99C-5150	150 ± 7.5	30 ± 3
SMD-99C-5175	175 ± 8	35 ± 4
SMD-99C-5200	200 ± 10	40 ± 4
SMD-99C-5250	250 ± 12.5	50 ± 5
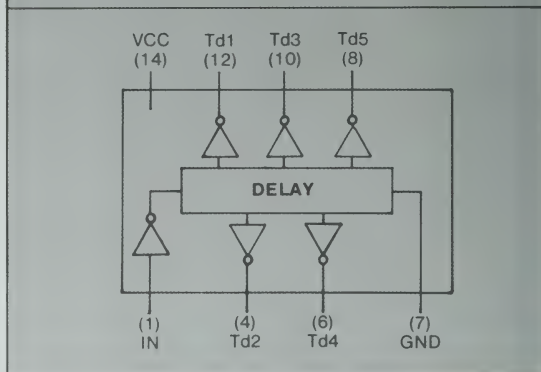
Fast Logic
Surface Mounted
Delay Line
SERIES: SMD-99F
TTL Interfaced

data delay devices, inc. ®

Features

■ Designed for surface mounting.
■ Low profile .175 max. height.
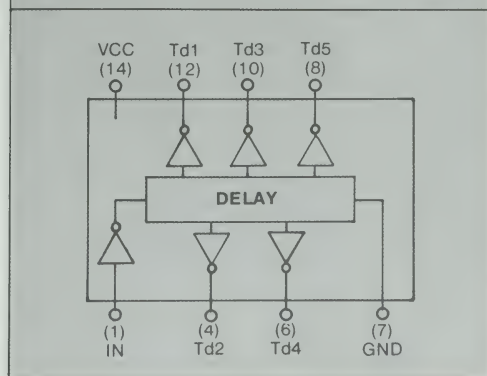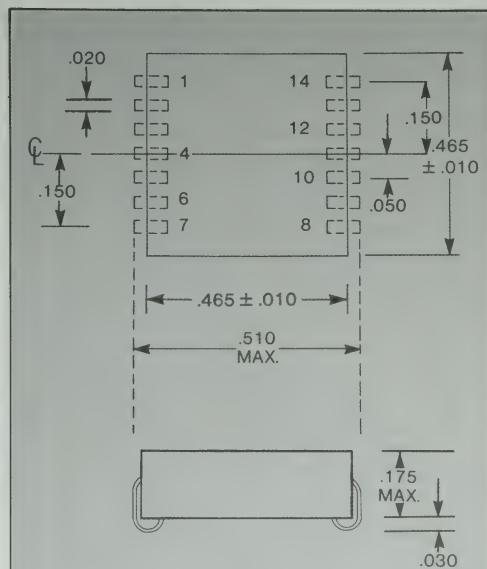■ Completely interfaced for TTL.
■ Up to 5 outputs.
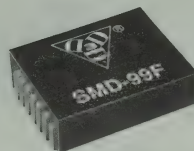
Specifications:

■ **Outputs:** 5, equally spaced.
■ **Delay tolerance:** see table.
■ **Rise-time:** 2 ns typ.
■ **Minimum pulse width:** 40% of total delay.
■ **Temperature range:** 0 to 70°C. (−55°C to + 125°C on request.)*
■ **Temperature coefficient:** 100 PPM/°C.
■ **Supply voltage:** 4.75 to 5.25 Vdc.
■ **Supply current:**
  I_{CCL}: 32 ma.
  I_{CCL}: 7 ma.
■ **DC parameters:** See TTL-Fast Schottky Logic
                    Table on Page 6.

*Add "M" after PART NO. Example: SMD-99F-5100M
Height is .225 max.

Part Number	Total Delay (ns)	Tap Delay (ns)
*SMD-99F-5004	4 ± 1	1 ± 0.5
*SMD-99F-5006	6 ± 1	1.5 ± 0.5
*SMD-99F-5008	8 ± 2	2 ± 1
*SMD-99F-5010	10 ± 2	2.5 ± 1
*SMD-99F-5012	12 ± 2	3 ± 1
*SMD-99F-5016	16 ± 2	4 ± 1.5
*SMD-99F-5020	20 ± 3	5 ± 2
SMD-99F-5025	25 ± 3	5 ± 2
SMD-99F-5030	30 ± 3	6 ± 2
SMD-99F-5035	35 ± 3	7 ± 2
SMD-99F-5040	40 ± 3	8 ± 2
SMD-99F-5045	45 ± 3	9 ± 3
SMD-99F-5050	50 ± 3	10 ± 3
SMD-99F-5060	60 ± 3	12 ± 3
SMD-99F-5075	75 ± 4	15 ± 3
SMD-99F-5100	100 ± 5	20 ± 3
SMD-99F-5125	125 ± 6.5	25 ± 3
SMD-99F-5150	150 ± 7.5	30 ± 3
SMD-99F-5175	175 ± 8	35 ± 4
SMD-99F-5200	200 ± 10	40 ± 4
SMD-99F-5250	250 ± 12.5	50 ± 5

*Time delay measured with respect to 1st tap.
3.5 ns ± 1 ns inherent delay.
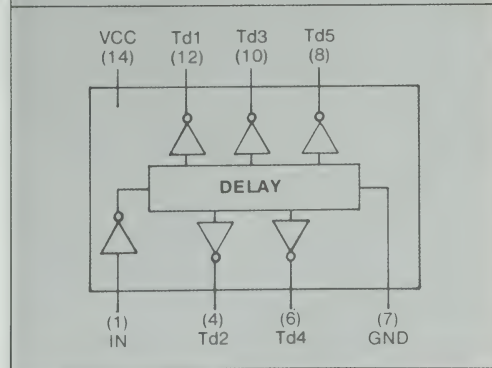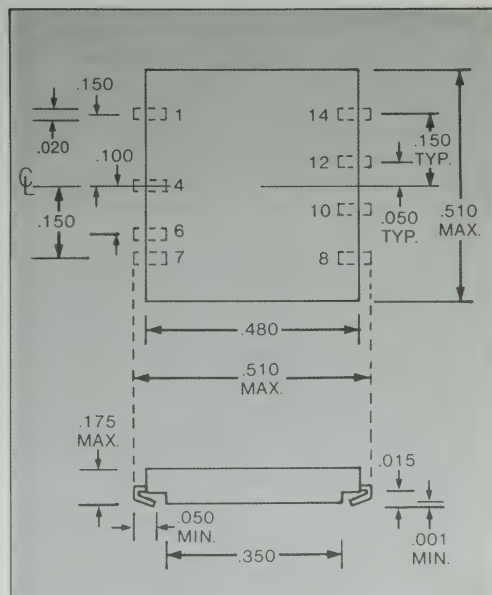
Multiple Digital Delay Units

SERIES: MDU-2F
(14 pins DIP) TTL Interfaced

data delay devices, inc.

Features:

- **Auto-insertable**
- **Completely interfaced for TTL & DTL application.**
- **P.C. board space economy achieved.**
- **Fits standard 14 pins DIP socket.**
- **2 equal delay units/package.**

Specifications:

- **Delay tolerance:** ±5% or 2 ns whichever is greater.
- **Rise-time:** 2 ns typically.
- **Temperature coefficient:** 100 PPM/°C.
- **Temperature range:** 0° to + 70°C.
- **Input pulse width:** Min. 100% of total delay.
- **Input rep. rate** = Min. 3 × pulse width.
- **Supply voltage:** 5 Vdc ± 5%.
- **Supply Current:**
  I_{CCL}: 54 ma.
  I_{CCH}: 12 ma.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Test Conditions:

- Input Pulse Width: >150% of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Rise-time is measured from .75 V to 2.4 V of leading time.
- All measurements made @ V_{cc}= 5V; T_A = +25°C; no loads on taps.

Part No.	Delay Per Line (ns)
MDU-2F-5	5
MDU-2F-10	10
MDU-2F-15	15
MDU-2F-20	20
MDU-2F-25	25
MDU-2F-30	30
MDU-2F-35	35
MDU-2F-40	40
MDU-2F-45	45
MDU-2F-50	50
MDU-2F-60	60
MDU-2F-75	75
MDU-2F-100	100
MDU-2F-125	125
MDU-2F-150	150
MDU-2F-200	200
MDU-2F-250	250

Other delay times available on request.

Lead Material:
Nickel-iron alloy 42
TIN PLATE
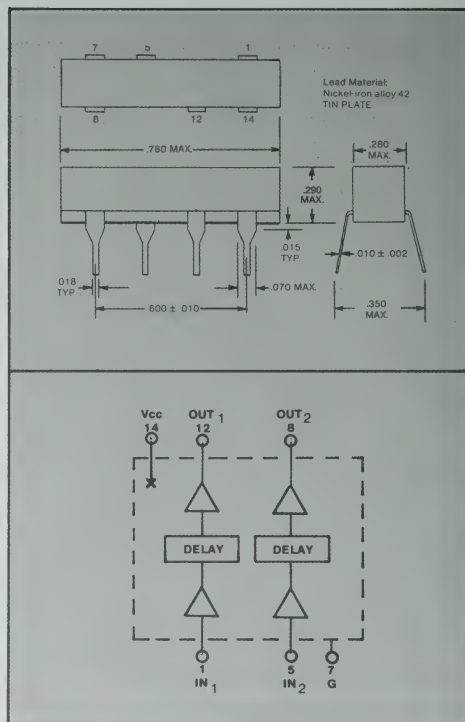
Multiple Digital Delay Units

SERIES: MDU-3F
(14 pins DIP) TTL Interfaced
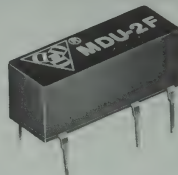
data delay devices, inc. ®

Features:

- **Auto-insertable.**
- **Completely interfaced for TTL & DTL application.**
- **P.C. board space economy achieved.**
- **Fits standard 14 pins DIP socket.**
- **3 equal delay units/package.**

Specifications:

- **Delay tolerance:** ±5% or 2 ns whichever is greater.
- **Rise-time:** 2 ns typically.
- **Temperature coefficient:** 100 PPM/°C.
- **Temperature range:** 0° to + 70°C.
- **Input pulse width:** Min. 100% of total delay.
- **Input rep. rate** = Min. 3 × pulse width.
- **Supply voltage:** 5 Vdc ± 5%.
- **Supply Current:**
  I_{CCL}: 74 ma.
  I_{CCH}: 14 ma.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Test Conditions:

- Input Pulse Width: >150% of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Rise-time is measured from .75 V to 2.4 V of leading time.
- All measurements made @ V_{CC}= 5V; T_A = +25°C, no loads on taps.

Part No.	Delay Per Line (ns)
MDU-3F-5	5
MDU-3F-10	10
MDU-3F-15	15
MDU-3F-20	20
MDU-3F-25	25
MDU-3F-30	30
MDU-3F-35	35
MDU-3F-40	40
MDU-3F-45	45
MDU-3F-50	50
MDU-3F-60	60
MDU-3F-75	75
MDU-3F-100	100

Other delay times available on request.
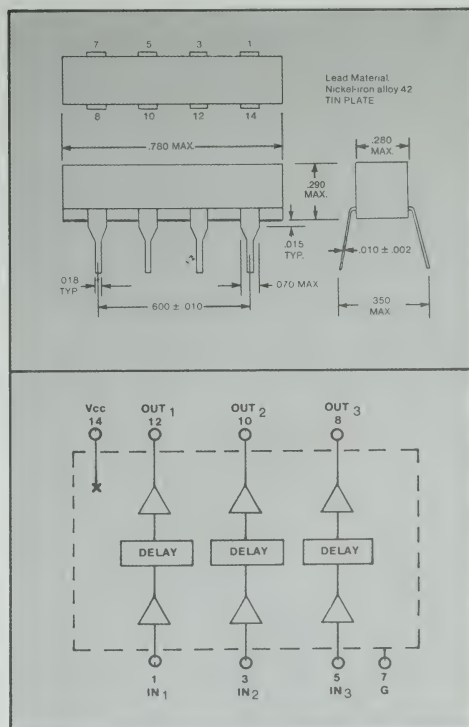
Fast Logic
Multiple Digital Delay Units
SERIES: MDU-4F
(14 pins DIP) TTL Interfaced

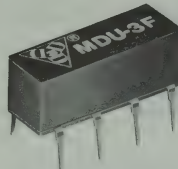**data delay devices, inc.** ®

Features:

- Completely interfaced for TTL & DTL application.
- P.C. board space economy achieved.
- Fits standard 14 pins DIP socket.
- 4 equal delay units/package.
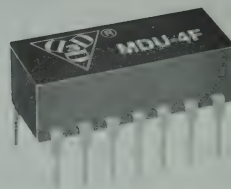
Specifications:

- **Delay Tolerance:** ±5% or 2 ns whichever is greater.
- **Rise-time:** 2 ns typically.
- **Temperature coefficient:** 100 PPM/°C.
- **Temperature range:** 0° to + 70°C.
- **Supply voltage:** 5 Vdc ± 5%.
- **Supply Current:**
  I_{CCL}: 110 ma.
  I_{CCH}: 24 ma.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Test Conditions:

- Input Pulse Width: ≥ 150% of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Rise-time is measured from .75 V to 2.4 V of leading time
- All measurements made @ V_{CC} = 5V; T_A = +25°C.

Part No.	Delay Per Line (ns)
MDU-4F-5	5
MDU-4F-10	10
MDU-4F-15	15
MDU-4F-20	20
MDU-4F-25	25
MDU-4F-30	30
MDU-4F-35	35
MDU-4F-40	40
MDU-4F-45	45
MDU-4F-50	50

Other delay times available on request.
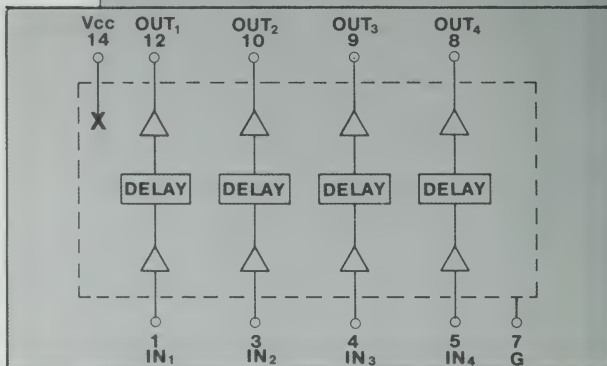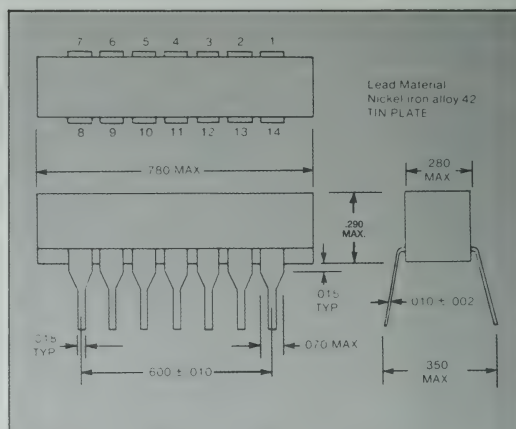
Lead Material
Nickel iron alloy 42
TIN PLATE

780 MAX
280 MAX
.290 MAX.
.015 TYP
.010 ± .002
.015 TYP
.070 MAX
600 ± .010
350 MAX

Vcc 14	OUT₁ 12	OUT₂ 10	OUT₃ 9	OUT₄ 8

X

DELAY DELAY DELAY DELAY

| 1 IN₁ | 3 IN₂ | 4 IN₃ | 5 IN₄ | 7 G |

Multiple Digital Delay Units

SERIES: MDU-12
(16 pins DIP) 10KH ECL Interfaced

data delay devices, inc.

Features:

- **Input & output buffered.**
- **2 delay lines/package.**
- **Fits in Standard 16 Pins DIP.**

Specifications:

- **Total Delay Tolerance:** ± 5% or better, or 2 ns whichever is greater.
- **Rise-time:** 2 ns typical.
- **Supply voltage:** −5.2V
- **Operating Temperature:** −30°C to 85°C.
- **Power Dissipation:** −200 mw typ. (no load).
- **Temperature coefficient:** 100 PPM/°C.
- **Fan-out:** 70 ECL loads.
- **DC parameters:** See ECL-10KH Logic Table on Page 6.

Test Conditions:

- **Input pulse-width:** 150% of total delay.
- **Input pulse rise-time:** ≤6 ns.
- **Input pulse voltage:** −.7V
- **Rise-time measured from 20% to 80% of leading edge.**
- **Delay time measured at 50% of leading edge.**
- **All measurements taken @ V_{EE} = −5.2V and T_A = 25°C.**

† or case stand-offs

Part No.	Delay Per Line (ns)
MDU-12-5	5
MDU-12-10	10
MDU-12-15	15
MDU-12-20	20
MDU-12-25	25
MDU-12-30	30
MDU-12-35	35
MDU-12-40	40
MDU-12-45	45
MDU-12-50	50
MDU-12-60	60
MDU-12-75	75
MDU-12-100	100
MDU-12-125	125
MDU-12-150	150
MDU-12-200	200
MDU-12-250	250

Other delay times on request.
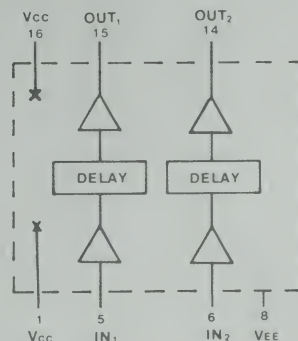
Multiple Digital Delay Units

SERIES: MDU-13
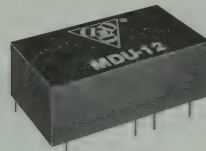### (16 pins DIP) 10KH ECL Interfaced

data delay devices, inc. ®

Features:

- Input & Output Buffered.
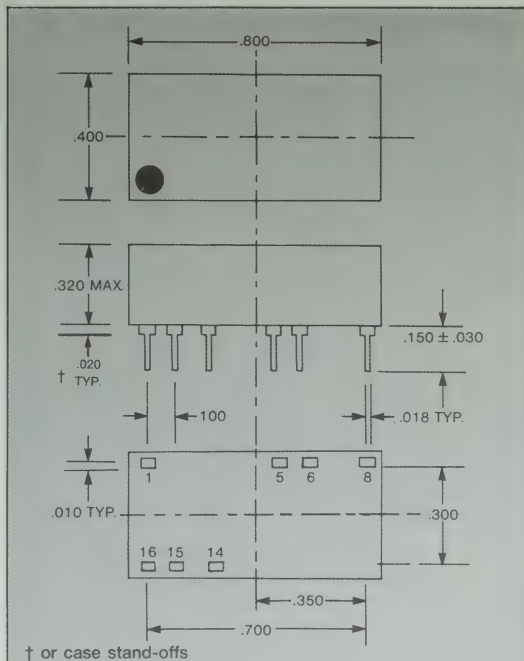- 3 Delay lines/package.
- Fits in Standard 16 Pins DIP.

Specifications:

- **Total Delay Tolerance:** ± 5% or better, or 2 ns whichever is greater.
- **Rise-time:** 2 ns typical.
- **Supply voltage:** −5.2V
- **Operating Temperature:** −30°C to 85°C.
- **Power Dissipation:** −200 mw typ. (no load).
- **Temperature coefficient:** 100 PPM/°C.
- **Fan-out:** 70 ECL loads.
- **DC parameters:** See ECL-10KH Logic Table on Page 6.

Test Conditions:

- Input pulse-width: 150% of total delay.
- Input pulse rise-time: ≤6 ns.
- Input pulse voltage: −.7V
- Rise-time measured from 20% to 80% of leading edge.
- Delay time measured at 50% of leading edge.
- All measurements taken @ V_{EE} = −5.2V and T_A = 25°C.

Part No.	Delay Per Line (ns)
MDU-13-5	5
MDU-13-10	10
MDU-13-15	15
MDU-13-20	20
MDU-13-25	25
MDU-13-30	30
MDU-13-35	35
MDU-13-40	40
MDU-13-45	45
MDU-13-50	50

Other delay times on request.

† or case stand-offs
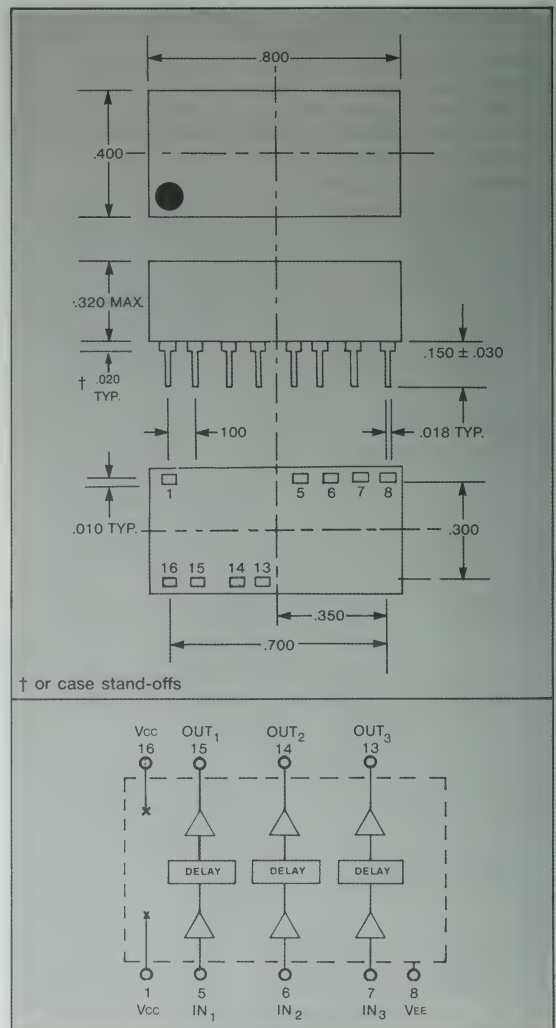
Multiple Digital Delay Units

SERIES: MDU-14
(24 pins DIP) 100K ECL Interfaced

Features:

- Input & output buffered.
- 4 delay lines/package.
- Compatible with ECL circuits.

Specifications:

- **Total delay tolerance:** ±5% or 1 ns whichever is greater.
- **Rise time:** 1 ns typ.
- **Input pulse width:** 40% of total delay.
- **Input PRR:** 3 × PW.
- **Input pulse voltage:** .8V p-p (−.9V to −1.7V).
- **Supply Voltage (Vee):** −5V.
- **Supply current (Vee):** 100 ma typ.
- **Operating temperature:** 0°C to +85°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Fan-out capabilities:** 70 ECL loads.
- **DC parameters:** See ECL-100K Logic Table on Page 6.
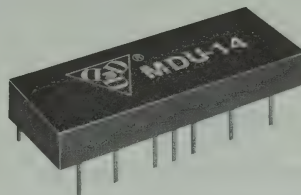
Part No.	Delay Per Line (ns)
MDU-14-2	2
MDU-14-2.5	2.5
MDU-14-3	3
MDU-14-4	4
MDU-14-5	5
MDU-14-6	6
MDU-14-7	7
MDU-14-8	8
MDU-14-9	9
MDU-14-10	10
MDU-14-12.5	12.5
MDU-14-15	15
MDU-14-20	20
MDU-14-25	25

Other delay times on request.
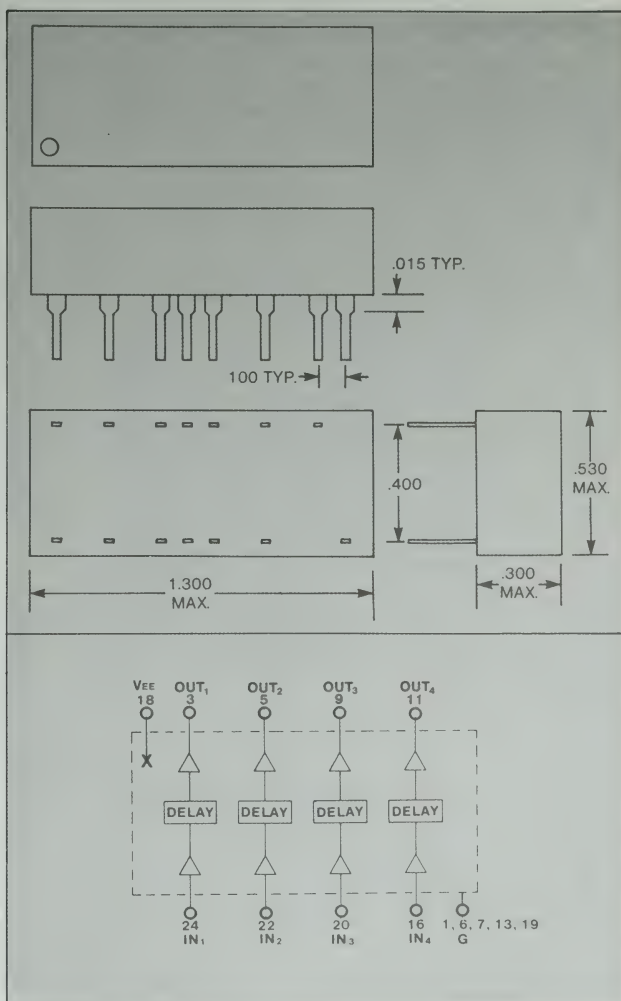
Fast Logic

Multiple Digital Delay Units

SERIES: MDU-28F
(8 pins DIP) TTL Interfaced

data delay devices, inc. ®

Features:

- ■ **Auto-insertable.**
- ■ **Low cost.**
- ■ **Completely interfaced for TTL.**
- ■ **Low profile.**
- ■ **Fits standard 8 pins DIP socket.**
- ■ **2 equal delay units/package.**

Specifications:

- ■ **Delay Tolerance:** See table.
- ■ **Rise-time:** 2 ns typically.
- ■ **Temperature coefficient:** 100 PPM/°C.
- ■ **Temperature range:** 0° to + 70°C.
- ■ **Input pulse width:** Min. 100% of total delay.
- ■ **Input rep. rate:** Min. 3 × pulse width.
- ■ **Supply voltage:** 5 Vdc ± 5%.
- ■ **Supply Current:**
  I_{CCL}: 54 ma.
  I_{CCH}: 12 ma.
- ■ **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Test Conditions:

- ■ Input Pulse Width: >150% of total delay.
- ■ Time delay measured @ 1.5 V on rising edge.
- ■ Rise-time is measured from .75 V to 2.4 V of leading time.
- ■ All measurements made @ V_{cc}= 5V; T_A= +25°C; no loads on taps.

Part No.	Delay Per Line (ns)
MDU-28F-6	6 ± 1
MDU-28F-8	8 ± 2
MDU-28F-10	10 ± 2
MDU-28F-12	12 ± 2
MDU-28F-16	16 ± 2
MDU-28F-20	20 ± 3
MDU-28F-30	30 ± 3
MDU-28F-35	35 ± 3
MDU-28F-40	40 ± 3
MDU-28F-45	45 ± 3
MDU-28F-50	50 ± 3
MDU-28F-60	60 ± 3
MDU-28F-75	75 ± 4
MDU-28F-100	100 ± 5
MDU-28F-125	125 ± 6.5
MDU-28F-150	150 ± 7.5
MDU-28F-175	175 ± 8
MDU-28F-200	200 ± 10
MDU-28F-250	250 ± 12.5

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.500
.280 MAX.
.290 MAX.
.015 TYP.
.010 ± .002
.018 TYP.
.070 MAX.
.300
.350 MAX.
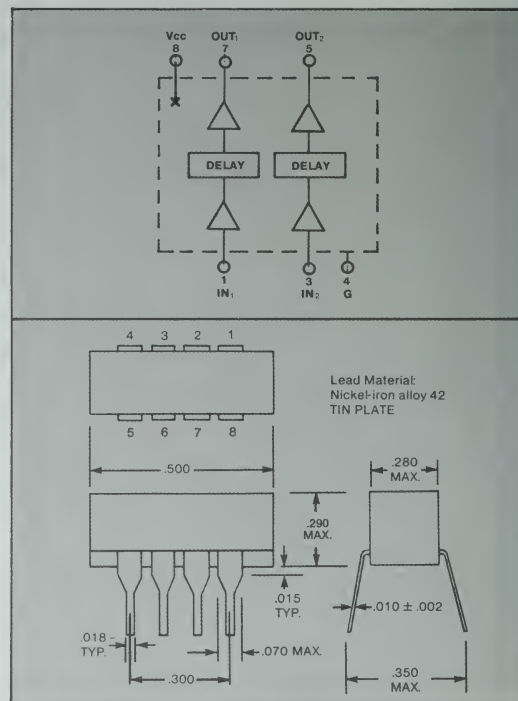
Fast Logic
Multiple Digital Delay Units

SERIES: MDU-38F
(8 pins DIP) TTL Interfaced

data delay devices, inc.

Features:

- Auto-insertable.
- Completely interfaced for TTL & DTL application.
- P.C. board space economy achieved.
- Fits standard 8 pins DIP socket.
- 3 equal delay units/package.

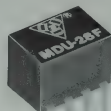## Specifications:

- **Delay Tolerance:** ±5% or 2 ns whichever is greater.
- **Rise-time:** 2 ns typically.
- **Temperature coefficient:** 100 PPM/°C.
- **Temperature range:** 0° to + 70°C.
- **Input pulse width:** Min. 100% of total delay
- **Input rep. rate** = Min. 3 × pulse width.
- **Supply voltage:** 5 Vdc ± 5%.
- **Supply Current:**
  I_{CCL}: 74 ma.
  I_{CCH}: 14 ma.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Test Conditions:

- Input Pulse Width: > 150% of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Rise-time is measured from .75 V to 2.4 V of leading time.
- All measurements made @ V_{cc} = 5V; T_A = +25°C, no loads on taps.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

Part No.	Delay Per Line (ns)	Part No.	Delay Per Line (ns)
MDU-38F-5	5	MDU-38F-40	40
MDU-38F-10	10	MDU-38F-45	45
MDU-38F-15	15	MDU-38F-50	50
MDU-38F-20	20	MDU-38F-60	60
MDU-38F-25	25	MDU-38F-75	75
MDU-38F-30	30	MDU-38F-100	100
MDU-38F-35	35		

Other delay times available on request.
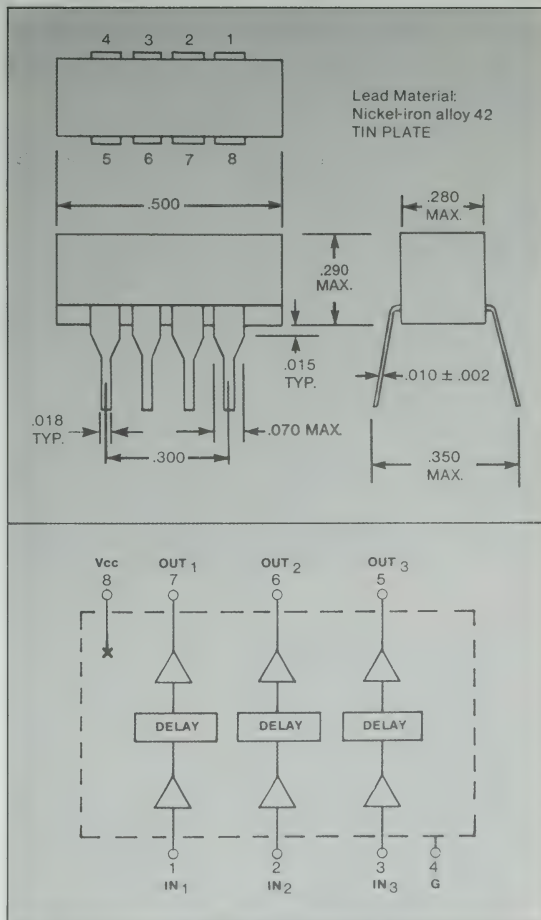
Timing Definition For Programmable Delay Lines (PDU's)

A diagram with signals labeled $A_1 - A_N$, EN, IN, OUT, showing timing markers T_{SUA}, T_{SUE}, PW_{IN}, T_{DO}, PW_{OUT}, T_{AR}, T_{ER}.
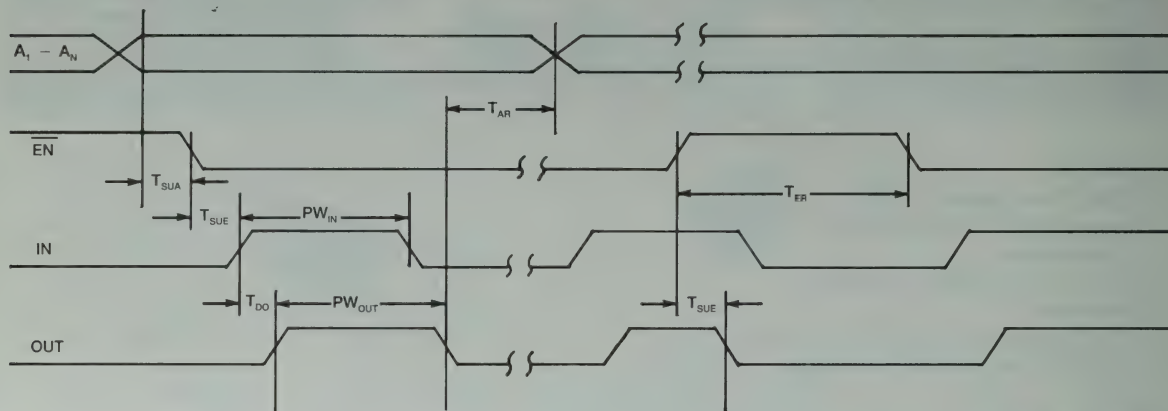
Typical Set-Up Specifications

Series	T_{SUA} (ns)	T_{SUE} (ns)	T_{DO} (ns)	Minimum Input Pulse-Width (ns)			Minimum Input Period (ns)
				*Absolute	*Suggested	Recommended	
PDU-13F	7	6	5.5	10% of T_{DT}	25% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-14F	7	6	9	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-15F	7	6	9	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-16F	7	6	9	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-17F	7	6	13	6% of T_{DT}	16% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-18F	7	6	13	6% of T_{DT}	16% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-53	2.9	–	2.2	10% of T_{DT}	25% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-54	2.9	–	3.3	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-108H	3.6	1.7	2.8	10% of T_{DT}	25% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-1016H	3.6	1.7	5.5	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-1032H	3.6	1.7	5.5	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-1064H	3.6	1.7	12	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-1316	12	12	17	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-1332	12	12	17	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-1364	12	12	15	8% of T_{DT}	20% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-10256H	3.2	1.7	12	6% of T_{DT}	16% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$
PDU-13256	12	12	20	6% of T_{DT}	16% of T_{DT}	Greater than T_{DT}	$2 \times PW_{IN}$

T_{SUA} = Address set-up time.
T_{SUE} = Enable set-up time.
PW_{IN} = Input pulse width.
PW_{OUT} = Output pulse width.
T_{DO} = Inherent delay time.

T_{AR} = Address recovery time.
T_{ER} = Enable recovery time.
T_{DT} = Total programmable delay time.

T_{ASEL} = Address selected time.
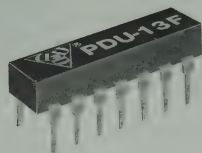$T_{AR} = T_{DO} + T_{DT} - T_{ASEL}$
$T_{ER} = T_{AR} + PW_{IN}$

Fast Logic
Programmable Delay Lines
SERIES: **PDU-13F**   (3 BIT) T²L Interfaced

data delay devices, inc. ®

Features:

- Digitally programmable in 8 delay steps.
- Fits standard 14 pins DIP socket.
- Input & outputs fully TTL interfaced & buffered.
- Two (2) separate outputs; inverting & non-inverting.
- Precise and stable delays.
- 10 T²L fan-out capability.
- Auto-insertable.

Specifications:

- **Delay variation:** Monotonic in one direction.
- **Total programmed delay tolerance:** 5% or 1 ns whichever is greater.
- **Inherent delay (T_{DO}):** 6 ns on pin 4 }
  5.5 ns on pin 5 } typical
- **Propagation delay:**
  Address to output (T_{SUA}) = 7 ns typ.
  Enable to output (T_{SUE}) = 6 ns typ.
- **Operating temperature:** 0° to 70° C.
- **Temperature coefficient:** 100 PPM/° C.
- **Supply voltage V_{CC}:** 5 Vdc ± 5%.
- **Supply current:** I_{CCH} = 20 ma.
  I_{CCL} = 45 ma.
- **Minimum pulse-width** = 20% of total delay.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.800 MAX.
.280 MAX.
.290 MAX.
.015 TYP.
.018 TYP.
.070 MAX.
.600 ± .010
.010 ± .002
.350 MAX.

ADDRESS

1 2 3 $\overline{E}_0$
10 9 8 6

V_{CC} 14
IN 1
GRD 7

DIGITAL DELAY

4 OUT
5 $\overline{OUT}$
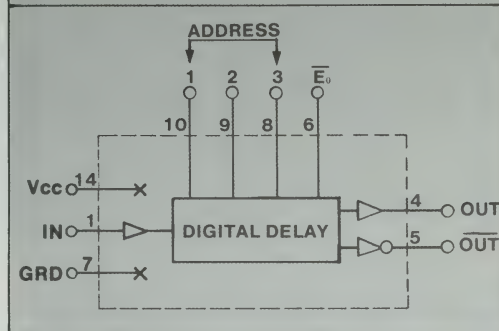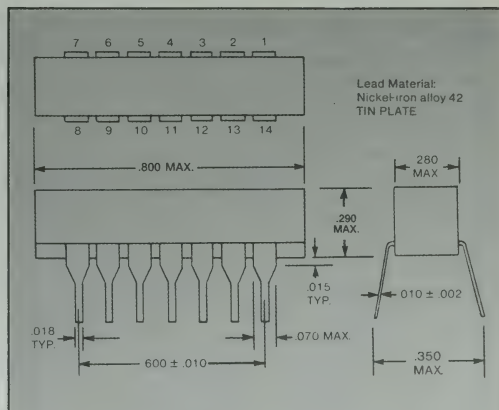
TRUTH TABLE

Enable	Address (Bit No.)			Delay Out
	3	2	1	
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	0	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	φ	φ	φ	0

1 = High
0 = Low
φ = Don't care
T_0 = Reference or inherent delay of circuit.
T_1 to T_7 = Multiplier of incremental delay.

Part Number	Incremental Delay Per Step (ns)		Total Delay* Change (ns)
PDU-13F-.5	.5	÷ .3	3.5
PDU-13F-1	1	÷ .4	7
PDU-13F-2	2	÷ .4	14
PDU-13F-3	3	− .5	21
PDU-13F-5	5	÷ .6	35
PDU-13F-10	10	÷ 1.0	70
PDU-13F-15	15	÷ 1.3	105
PDU-13F-20	20	− 1.5	140
PDU-13F-40	40	÷ 2.0	280
PDU-13F-50	50	÷ 2.5	350

*This delay value does not include T_0 delay.

3 Mt. Prospect Avenue, Clifton, New Jersey 07013 ■ (201) 773-2299 ■ FAX (201) 773-9672 ■ TWX 710-989-7008

Fast Logic

Programmable Delay Units

SERIES: PDU-14F   (4 Bit) TTL Interfaced

data delay devices, inc.

Features:

- **Input & Output TTL buffered**
- **4-Bit TTL programmable delay line**
- **Two (2) Separate outputs; inverting and non-inverting.**
- **Completely interfaced**
- **Compact & low profile**

Specifications:

- Delay variation: Monotonic in one direction.
- Programmed delay tolerance: 5% or 1 ns whichever is greater.
- Inherent delay (T_{DO}): 9 ns on pin 2 } 8 ns on pin 1 } typical
- Propagation delay:
  Address to output (T_{SUA}) = 7 ns typ.
  Enable to output (T_{SUE}) = 6 ns typ.
- Supply voltage: 5 Vdc ± 5%.
- Operating temperature: 0-70° C.
- Temperature coefficient: 100 PPM/° C.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.

- Supply current: I_{CCH} = 30 ma.
  I_{CCL} = 74 ma.
- Minimum pulse-width = 10% of total delay.

Test Conditions:

- Input pulse-width:
  > 150% of Max. delay.
- Input pulse spacing:
  > 3 times of Max. delay.
- Input pulse voltage:
  TTL logic.
- Measurements taken @ T_a = 25°C; Vcc = 5V.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

1.270
.280 MAX.
.290 MAX.
.015 TYP
.010 ± .002
.018 TYP
1.100
.070 MAX.
.350 MAX.

DELAY NETWORK

ADDRESS

Vcc IN GRD OUT OUT

TRUTH TABLE

Enable ($\overline{E_0}$)	Address				Delay Out
	4	3	2	1	
0	0	0	0	0	T_0
0	0	0	0	1	T_1
0	0	0	1	0	T_2
0	0	0	1	1	T_3
0	0	1	0	0	T_4
0	0	1	0	1	T_5
0	0	1	1	0	T_6
0	0	1	1	1	T_7
0	1	0	0	0	T_8
0	1	0	0	1	T_9
0	1	0	1	0	T_{10}
0	1	0	1	1	T_{11}
0	1	1	0	0	T_{12}
0	1	1	0	1	T_{13}
0	1	1	1	0	T_{14}
0	1	1	1	1	T_{15}
1	∅	∅	∅	∅	0

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-14F-.5	.5 ± .3	7.5
PDU-14F-1	1 ± .5	15
PDU-14F-2	2 ± .5	30
PDU-14F-3	3 ± 1.0	45
PDU-14F-4	4 ± 1.0	60
PDU-14F-5	5 ± 1.0	75
PDU-14F-6	6 ± 1.0	90
PDU-14F-8	8 ± 1.0	120
PDU-14F-10	10 ± 1.5	150
PDU-14F-12	12 ± 1.5	180
PDU-14F-15	15 ± 1.5	225
PDU-14F-20	20 ± 2.0	300
PDU-14F-25	25 ± 2.5	375
PDU-14F-30	30 ± 3.0	450
PDU-14F-35	35 ± 3.5	525
PDU-14F-40	40 ± 4.0	600
PDU-14F-45	45 ± 4.5	675
PDU-14F-50	50 ± 5.0	750
PDU-14F-60	60 ± 6.0	900
PDU-14F-80	80 ± 8.0	1,200
PDU-14F-100	100 ± 10.0	1,500

0 = Logic 0   1 = Logic 1   ∅ = Don't care.
T_0 = Reference or inherent delay of unit.
$T_1 \rightarrow T_{15}$ = Multiplier of incremental delay.

3 Mt. Prospect Avenue, Clifton, New Jersey 07013 ■ (201) 773-2299 ■ FAX (201) 773-9672 ■ TWX 710-989-7008

Fast Logic
Programmable Delay Units
SERIES: PDU-15F   (5 Bit) TTL Interfaced

data delay devices, inc. ®

Features:

- Input & Output TTL buffered
- 5-Bit TTL programmable delay line
- Two (2) Separate outputs; inverting and non-inverting.
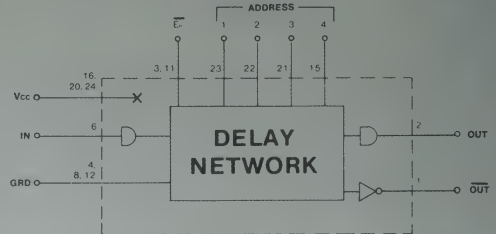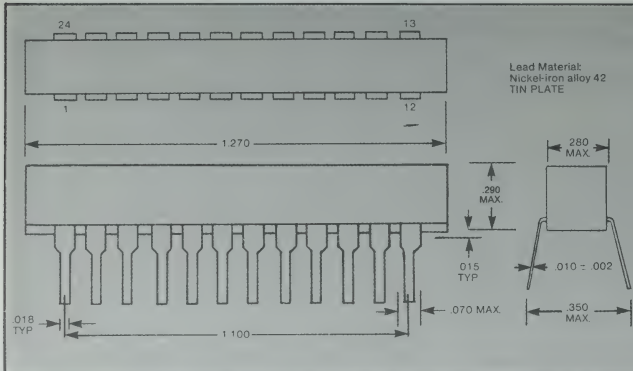- Completely interfaced
- Compact & low profile

Specifications:

- Propagation delay:
  Address to output (T_{SUA}) = 7 ns typ.
  Enable to output (T_{SUE}) = 6 ns typ.
- Delay variation: Monotonic in one direction.
- Programmed delay tolerance: ±5% or 1 ns whichever is greater.
- Inherent delay (T_{DO}): 9 ns on pin 2 } typical
  8 ns on pin 1 }
- Supply voltage: 5 Vdc ± 5%.
- Operating temperature: 0-70° C.
- Temperature coefficient: 100 PPM/° C.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.

- Supply current: I_{CCH} = 30 ma.
  I_{CCL} = 70 ma.
- Minimum pulse-width = 10% of total delay.

Test Conditions:

- Input pulse-width:
  > 150% of Max. delay.
- Input pulse spacing:
  > 3 times of Max. delay.
- Input pulse voltage:
  TTL logic.
- Measurements taken @
  T_a = 25°C; V_{CC} = 5V.

TRUTH TABLE

Enable (E₀)	Address					Delay Out
	5	4	3	2	1	
0	0	0	0	0	0	T_0
0	0	0	0	0	1	T_1
0	0	0	0	1	0	T_2
0	0	0	0	1	1	T_3
0	0	0	1	0	0	T_4
0	0	0	1	0	1	T_5
0	0	0	1	1	0	T_6
0	0	0	1	1	1	T_7
0	0	1	0	0	0	T_8
0	0	1	1	1	1	T_{15}
0	1	0	0	0	0	T_{16}
0	1	1	1	1	1	T_{31}
1	Ø	Ø	Ø	Ø	Ø	0

0 = Logic 0   1 = Logic 1   Ø = Don't care.
T_0 = Reference or inherent delay of unit.
T_1 → T_{31} Multiplier of incremental delay.

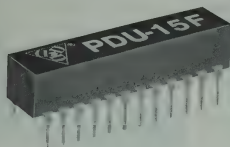| Part No.	Incremental Delay Per Step (ns)		Total Programmed Delay (ns)
PDU-15F-0.5	0.5	÷ 0.3	15.5
PDU-15F-1	1	÷ 0.5	31
PDU-15F-2	2	÷ 0.5	62
PDU-15F-3	3	÷ 1.0	93
PDU-15F-4	4	÷ 1.0	124
PDU-15F-5	5	÷ 1.0	155
PDU-15F-6	6	÷ 1.0	186
PDU-15F-8	8	÷ 1.0	248
PDU-15F-10	10	÷ 1.5	310
PDU-15F-12	12	÷ 1.5	372
PDU-15F-15	15	÷ 1.5	465
PDU-15F-20	20	÷ 2.0	620

=== Fast Logic

Programmable Delay Units

SERIES: PDU-16F (6-Bit) TTL Interfaced

data delay devices, inc. ®

Features:

- Input & Output TTL buffered
- 6-Bit TTL programmable delay line
- Two (2) Separate outputs; inverting and non-inverting.
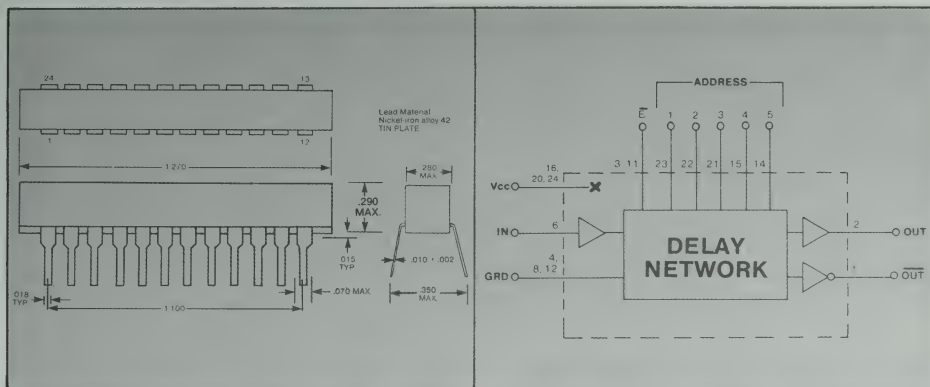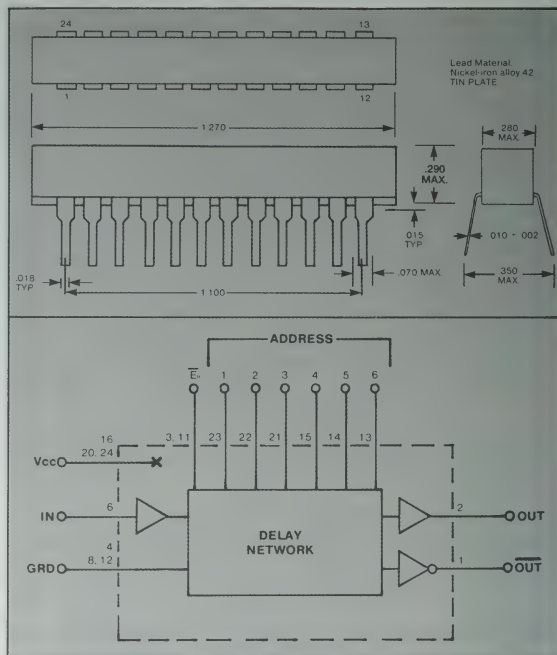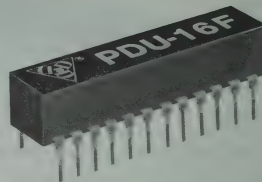- Completely interfaced
- Compact & low profile

Test Conditions:

- **Input pulse-width:** > 150% of Max. delay.
- **Input pulse spacing:** > 3 times of Max. delay.
- **Input pulse voltage:** TTL logic.
- **Measurements taken @** $T_a = 25°C$; $V_{cc} = 5V$.

Specifications:

- **Propagation delay:**
  Address to output $(T_{SUA}) = 7$ ns typ.
  Enable to output $(T_{SUE}) = 6$ ns typ.
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ±5% or 1 ns whichever is greater.
- **Inherent delay (T_{DO}):** 9 ns on pin 2 } typical
                                  8 ns on pin 1 }
- **Supply voltage:** 5 Vdc ± 5%.
- **Operating temperature:** 0-70° C.
- **Temperature coefficient:** 100 PPM/° C.
- **Supply current:** $I_{CCH} = 30$ ma.
                      $I_{CCL} = 74$ ma.
- **Minimum pulse-width** = 10% of total delay.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

TRUTH TABLE

Enable (E₀)	Address						Delay Out
	6	5	4	3	2	1	
0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	1	T_1
0	0	0	0	0	1	0	T_2
0	0	0	0	0	1	1	T_3
0	0	0	0	1	0	0	T_4
0	0	0	0	1	0	1	T_5
0	0	0	0	1	1	0	T_6
0	0	0	0	1	1	1	T_7
0	0	0	1	0	0	0	T_8
0	0	0	1	1	1	1	T_{15}
0	0	1	0	0	0	0	T_{16}
0	0	1	1	1	1	1	T_{31}
0	1	0	0	0	0	0	T_{32}
0	1	1	1	1	1	1	T_{63}
1	∅	∅	∅	∅	∅	∅	0

0 = Logic 0   1 = Logic 1   ∅ = Don't care.
T_0 = Reference or inherent delay of unit.
$T_1 \rightarrow T_{63}$ Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-16F-0.5	0.5 ÷ 0.3	31.5
PDU-16F-1	1 ± 0.5	63
PDU-16F-2	2 ± 0.5	126
PDU-16F-3	3 ± 1.0	189
PDU-16F-4	4 ± 1.0	252
PDU-16F-5	5 ± 1.0	315
PDU-16F-6	6 ± 1.0	378
PDU-16F-8	8 ± 1.0	504
PDU-16F-10	10 ± 1.5	630

Fast Logic
Programmable Delay Units
SERIES: PDU-17F
(7 Bit) TTL Interfaced

data delay devices, inc. ®

Specifications:

- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ±5% or 2 ns whichever is greater.
- **Inherent delay (T_{DO}):** 13 ns on pin 3 ⎫ typical / 12 ns on pin 2 ⎭
- **Propagation delay:**
  Address to output (T_{SUA}) = 7 ns typ.
  Enable to output (T_{SUE}) = 6 ns typ.
- **Supply voltage:** 5 Vdc ± 5%.
- **Operating temperature:** 0-70° C.
- **Temperature coefficient:** 100 PPM/° C.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

- **Supply current:** I_{CCH} = 68 ma.
  I_{CCL} = 86 ma.
- **Minimum pulse-width** = 8% of total delay.

Test Conditions:
- **Input pulse-width:** > 150% of Max. delay.
- **Input pulse spacing:** > 3 times of Max. delay.
- **Input pulse voltage:** TTL logic.
- **Measurements taken @** Ta = 25°C; Vcc = 5V.

Features:
- **Input & Output TTL buffered**
- **7-Bit TTL programmable delay line**
- **Two (2) Separate outputs; inverting and non-inverting.**
- **Completely interfaced**
- **Compact & low profile**
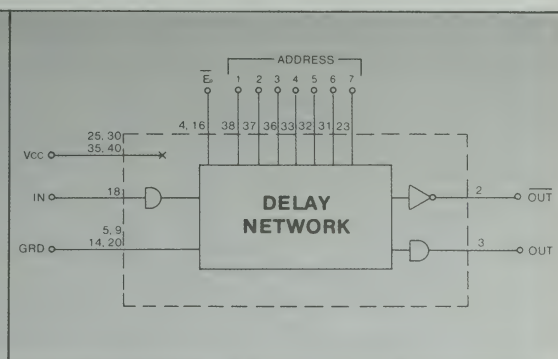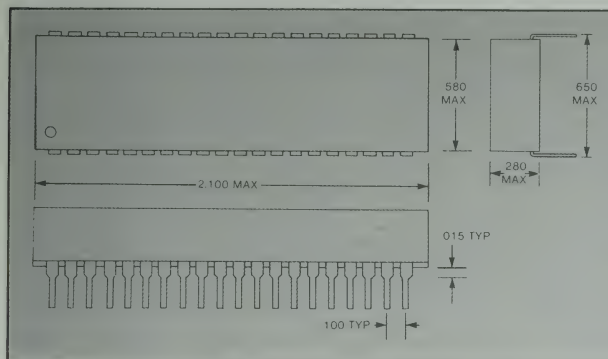
TRUTH TABLE

7	6	5	4	3	2	1	Enable (E_0)	Delay Out
0	0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	1	0	T_1
0	0	0	0	0	1	0	0	T_2
0	0	0	0	0	1	1	0	T_3
0	0	0	0	1	0	0	0	T_4
0	0	0	0	1	1	1	0	T_7
0	0	0	1	0	0	0	0	T_8
0	0	0	1	1	1	1	0	T_{15}
0	0	1	0	0	0	0	0	T_{16}
0	0	1	1	1	1	1	0	T_{31}
0	1	0	0	0	0	0	0	T_{32}
0	1	1	1	1	1	1	0	T_{63}
1	0	0	0	0	0	0	0	T_{64}
1	1	1	1	1	1	1	0	T_{127}
∅	∅	∅	∅	∅	∅	∅	1	0

0 = Logic 0   1 = Logic 1   ∅ = Don't care.
T_0 = Reference or inherent delay of unit.
$T_1 \rightarrow T_{255}$ multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-17F-.5	.5 ÷ .3	63.5
PDU-17F-1	1 - .5	127
PDU-17F-2	2 - .5	254
PDU-17F-3	3 - 1.0	381
PDU-17F-4	4 - 1.0	508
PDU-17F-5	5 - 1.5	635
PDU-17F-6	6 - 1.5	762
PDU-17F-7	7 - 1.5	889
PDU-17F-8	8 - 2.0	1,016
PDU-17F-9	9 - 2.0	1,143
PDU-17F-10	10 - 2.0	1,270

NOTE: 1. For the sake of simplicity all 128 programmable steps are not shown in this truth table.

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Programmable Delay Units

SERIES: PDU-18F (8 Bit) TTL Interfaced

data delay devices, inc. ®

Features:
- Input & Output TTL buffered
- 8-Bit TTL programmable delay line
- Two (2) Separate outputs; inverting and non-inverting.
- Completely interfaced
- Compact & low profile

Specifications:
- Delay variation: Monotonic in one direction.
- Programmed delay tolerance: ±5% or 2 ns whichever is greater.
- Inherent delay (T_{DO}): 19 ns on pin 3 } typical
  18 ns on pin 2
- Propagation delay:
  Address to output (T_{SUA}) = 7 ns typ.
  Enable to output (T_{SUE}) = 6 ns typ.
- Supply voltage: 5 Vdc ± 5%.
- Operating temperature: 0-70° C.
- Temperature coefficient: 100 PPM/° C.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.

- Supply current: I_{CCH} = 65 ma.
  I_{CCL} = 128 ma.
- Minimum pulse-width = 6% of total delay.

Test Conditions:
- Input pulse-width:
  > 150% of Max. delay.
- Input pulse spacing:
  > 3 times of Max. delay.
- Input pulse voltage:
  TTL logic.
- Measurements taken @
  Ta = 25°C; Vcc = 5V.

TRUTH TABLE

Address (Bit No.)								Enable (E_0)	Delay Out
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**		
0	0	0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	0	1	0	T_1
0	0	0	0	0	0	1	0	0	T_2
0	0	0	0	0	0	1	1	0	T_3
0	0	0	0	0	1	0	0	0	T_6
0	0	0	0	0	1	1	1	0	T_7
0	0	0	0	1	0	0	0	0	T_8
0	0	0	0	1	1	1	1	0	T_{15}
0	0	0	1	0	0	0	0	0	T_{16}
0	0	0	1	1	1	1	1	0	T_{31}
0	0	1	0	0	0	0	0	0	T_{32}
0	0	1	1	1	1	1	1	0	T_{63}
0	1	0	0	0	0	0	0	0	T_{64}
0	1	1	1	1	1	1	1	0	T_{127}
1	0	0	0	0	0	0	0	0	T_{128}
1	1	1	1	1	1	1	1	0	T_{235}
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	0

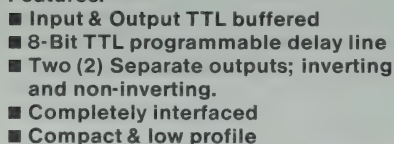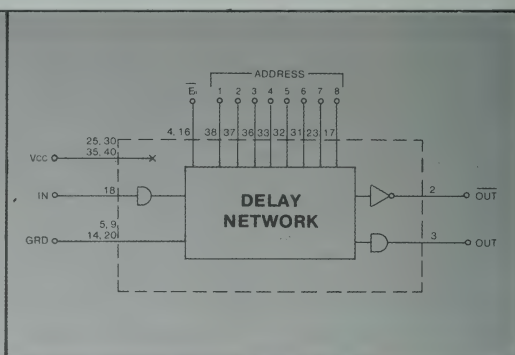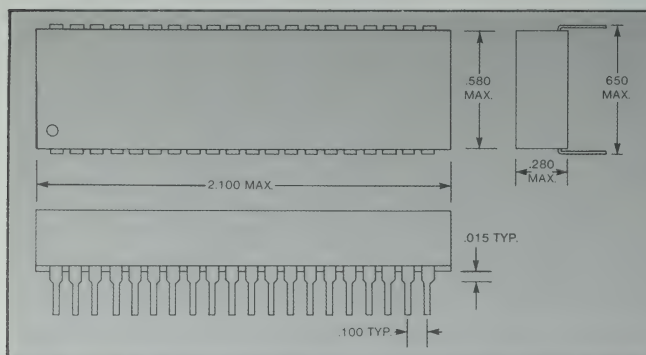0 = Logic 0   1 = Logic 1   Ø = Don't care.
T_0 = Reference or inherent delay of unit.
T_1 T_{255} Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-18F-.5	.5 ± .3	127.5
PDU-18F-1	1 ± .5	255
PDU-18F-2	2 ± .5	510
PDU-18F-3	3 ± 1.0	765
PDU-18F-4	4 ± 1.0	1,020
PDU-18F-5	5 ± 1.5	1,275
PDU-18F-6	6 ± 1.5	1,530
PDU-18F-7	7 ± 1.5	1,785
PDU-18F-8	8 ± 2.0	2,040
PDU-18F-9	9 ± 2.0	2,295
PDU-18F-10	10 ± 2.0	2,550

NOTE: 1. For the sake of simplicity all 256 programmable steps are not shown in this truth table.

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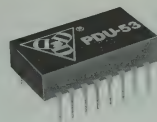# Programmable Delay Lines

SERIES: PDU-53

100K ECL Interfaced (3 BIT) 16 Pins DIP

data delay devices, inc. ®

Features:

- 3-BIT Programmable
- Accurate Timing
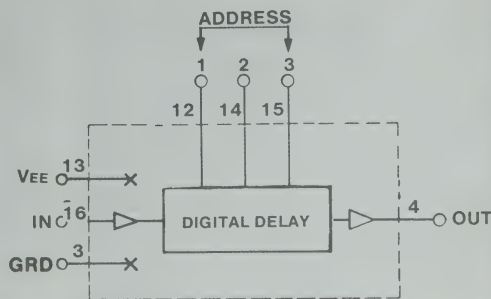- Completely 100K ECL Interfaced

Specifications:

- **Min. input pulse width:** 3 ns or 15% of total delay whichever is greater.
- **Min. PRR:** 8 ns or 2 × pulse width whichever is greater.
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** 5% or 40 ps whichever is greater.
- **Inherent delay (T_{DO}):** 2.2 ns.
- **Address to output prop. delay (T_{SUA}):** 2.9 ns max.
- **Power supply voltage:** -4.5V.
- **Power supply current:** -150 ma.
- **Temperature coefficient:** 100 PPM/°C.
- **Operating temp. range:** 0°C to $+85$°C.
- **Storage temp. range:** -65°C to $+150$°C.
- **DC parameters:** See ECL-100K Logic Table on Page 6.

Test Conditions:

- **Input pulse width:** 10 ns
- **Input PRR:** 100 ns
- **Input pulse rise-time:** 1 ns
- **Input pulse voltage:** .8V p-p
- **Supply voltage (V_{EE}):** -4.5V
- **Ambient temperature(T_a):** $+25$°C
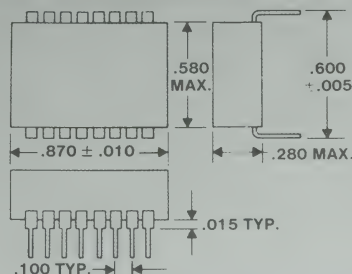
Part No.	Delay Increment (ps)	Total Programmed Delay (ps)
PDU-53-100	100 ± 50	700
PDU-53-200	200 ± 60	1,400
PDU-53-250	250 ± 60	1,750
PDU-53-400	400 ± 80	2,800
PDU-53-500	500 ± 100	3,500
PDU-53-750	750 ± 100	5,250
PDU-53-1000	1,000 ± 200	7,000
PDU-53-1200	1,200 ± 200	8,400
PDU-53-1500	1,500 ± 200	10,500
PDU-53-2000	2,000 ± 400	14,000
PDU-53-2500	2,500 ± 400	17,500
PDU-53-3000	3,000 ± 500	21,000

Programmable Delay Lines
SERIES: PDU-54

**100K ECL Interfaced (4 BIT) 24 Pins DIP**

data delay devices, inc.

Features:

- **4-BIT Programmable**
- **Accurate Timing**
- **Completely 100K ECL Interfaced**

Specifications:

- Min. input pulse width: 3 ns or 10% of total delay whichever is greater.
- Min. PRR: 8 ns or 2 × pulse width whichever is greater.
- Delay variation: Monotonic in one direction.
- Programmed delay tolerance: 5% or 40 ps whichever is greater.
- Inherent delay (T_{DO}): 3.3 ns.
- Address to output prop. delay (T_{SUA}): 2.9 ns max.
- Power supply voltage: −4.5V.
- Power supply current: −300 ma.
- Temperature coefficient: 100 PPM/°C.
- Operating temp. range: 0°C to +85°C.
- Storage temp. range: −65°C to +150°C.
- DC parameters: See ECL-100K Logic Table on Page 6.
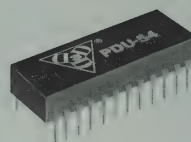
Test Conditions:

- Input pulse width: 10 ns
- Input PRR: 100 ns
- Input pulse rise-time: 1 ns
- Input pulse voltage: .8V p-p
- Supply voltage (V_{EE}): −4.5V
- Ambient temperature (T_a): +25°C
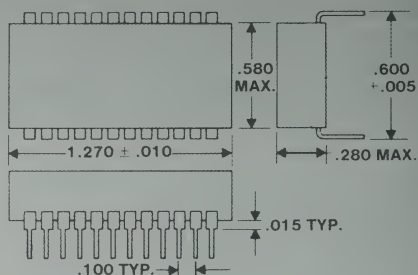
Part No.	Delay Increment (ps)	Total Programmed Delay (ns)
PDU-54-100	100 ± 50	1.50
PDU-54-200	200 ± 60	3.00
PDU-54-250	250 ± 60	3.75
PDU-54-400	400 ± 80	6.00
PDU-54-500	500 ± 100	7.50
PDU-54-750	750 ± 100	11.25
PDU-54-1000	1,000 ± 200	15.00
PDU-54-1200	1,200 ± 200	18.00
PDU-54-1500	1,500 ± 200	22.50
PDU-54-2000	2,000 ± 400	30.00
PDU-54-2500	2,500 ± 400	37.50
PDU-54-3000	3,000 ± 500	45.00
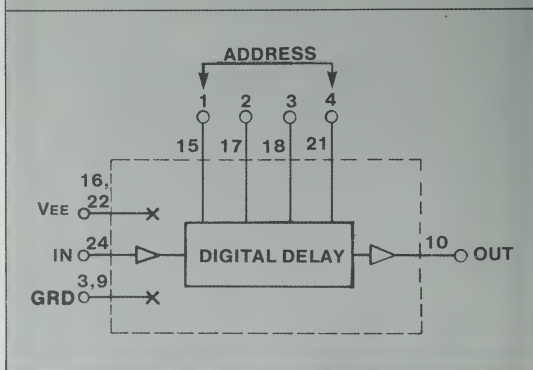
Programmable Delay Units
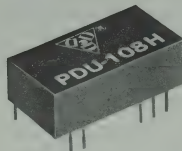
SERIES: PDU-108H

ECL Interfaced (3 BIT)

data delay devices, inc.

Features:

- Low propagation delay
- Digitally programmable in 8 delay steps.
- Delay increments of $1/2$ ns thru 50 ns.
- Fits standard 16 pins DIP socket.
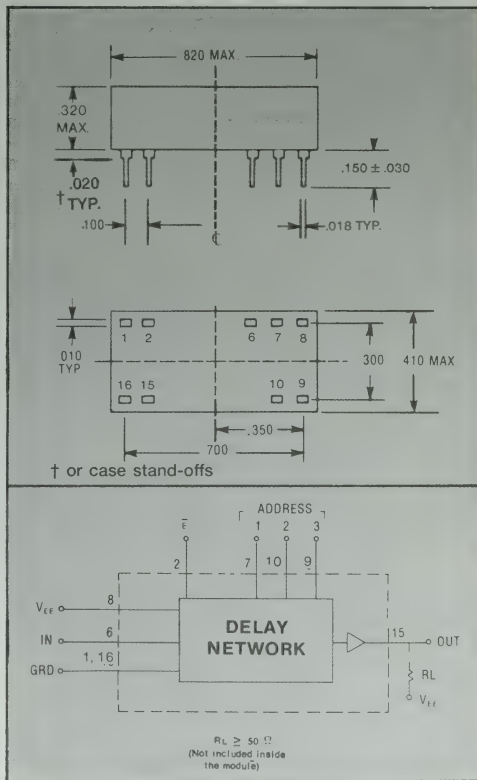- Output ECL interfaced.

Specifications:

- **Logic 1 input voltage:** $-.980$ V.
- **Logic 1 input current:** 10 ma.
- **Logic 0 input voltage:** -1.65 V.
- **Logic 0 input current:** -20 ma.
- **Logic 1 output voltage:** $-.96$ V.
- **Logic 0 output voltage:** -1.65 V.
- **Operating temperature:** 0° to 70°C.
- **Storage temperature:** $-55°$ to $+125°$C.
- **Power dissipation:** -290 mw typ. (no load).
- **Temperature coefficient:** 100 PPM/°C.
- **Delay variation:** Monotonic in one direction.
- **Total delay tolerance:** $\pm 5\%$ or 1 ns whichever is greater.
- **Inherent delay (T_{DO}):** 2.8 ns typ.
- **Propagation delay:**
  Address to output (T_{SUA}): $= 3.6$ ns typ.
  Enable to output (T_{SUE}): $= 1.7$ ns typ.

Test Conditions:

- **Input pulse-width:** 150% of total delay.
- **Input pulse rise-time:** ≥ 6 ns.
- **Input pulse voltage:** -1.5 V.
- **V_{EE} supply voltage:** -5 V.
- **V_{EE} supply current:** 56 ma typ.
- **Operating temperature:** 25°C.

† or case stand-offs

$RL \geq 50 \, \Omega$
(Not included inside the module)

TRUTH TABLE

Enable ($\overline{E_0}$)	Address (Bit No.) 3	2	1	Delay Out
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	∅	∅	∅	0

1 = High
0 = Low
∅ = Don't care
T_0 = Reference or inherent delay of circuit.
T_1 to T_7 = Multiplier of incremental delay.

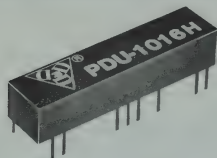| Part No.**	Min. Delay Increment (ns)		Total Delay* Change (ns)
PDU-108H-.5	.5	.3	3.5
PDU-108H-1	1	.4	7
PDU-108H-2	2	.4	14
PDU-108H-3	3	.5	21
PDU-108H-5	5	.6	35
PDU-108H-10	10	1	70
PDU-108H-20	20	1.5	140
PDU-108H-40	40	2	280
PDU-108H-50	50	2.5	350

*This delay value does not include the T_0 delay.
**Other delay increments available on request.

Digitally Programmable Delay Units
SERIES: PDU-1016H (4-Bit) ECL Interfaced

data delay devices, inc. ®

Specifications:
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ± 5% or 1 ns whichever is greater.
- **Inherent delay (T$_{DO}$):** 5.5 ns ± 1 ns for PDU-1016H-1 thru -5. Greater for rest of part numbers.
- **Propagation delay:**
  Address to output (T$_{SUA}$) = 3.6 ns typ.
  Enable to output (T$_{SUE}$) = 1.7 ns typ.
- **Power dissipation:** 615 mw typ.
- **Supply voltage:** −5 Vdc ± 5%.
- **Operating Temperature:** 0-70°C.
- **Temperature Coefficient:** 100 PPM/°C.
- **DC parameters:** See ECL-10KH Logic Table on Page 6.

Test Conditions
- **Input pulse-width:** ≥150% of Max. delay.
- **Input pulse spacing:** ≥3 times of Max. delay.
- **Input pulse voltage:** ECL logic.
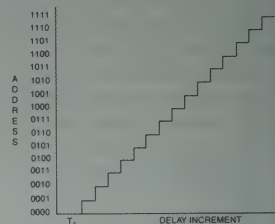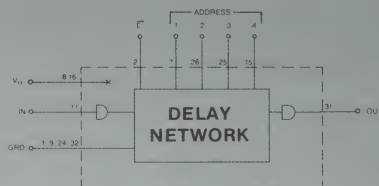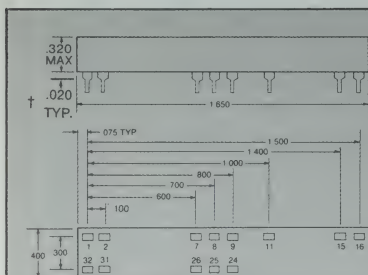- **Measurements taken @** Ta = 25°C, VEE = −5V.

Features:
- Low propagation delay
- Input & output ECL buffered
- 4-BIT ECL programmable delay line
- Output same polarity of input
- Completely interfaced
- Compact & low profile

† or case stand-offs

TRUTH TABLE

Enable (Ēo)	Address (Bit No.)				Delay Out
	4	3	2	1	
0	0	0	0	0	T$_0$
0	0	0	0	1	T$_1$
0	0	0	1	0	T$_2$
0	0	0	1	1	T$_3$
0	0	1	0	0	T$_4$
0	0	1	0	1	T$_5$
0	0	1	1	0	T$_6$
0	0	1	1	1	T$_7$
0	1	0	0	0	T$_8$
0	1	0	0	1	T$_9$
0	1	0	1	0	T$_{10}$
0	1	0	1	1	T$_{11}$
0	1	1	0	0	T$_{12}$
0	1	1	0	1	T$_{13}$
0	1	1	1	0	T$_{14}$
0	1	1	1	1	T$_{15}$
1	∅	∅	∅	∅	0

0 = Logic 0   1 = Logic 1   ∅ = Don't care.
T$_0$ = Reference or inherent delay of unit.
T$_1$ ⟶ T$_{15}$ = Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)		Total Programmed Delay (ns)
PDU-1016H-.5	.5	± .3	7.5
PDU-1016H-1	1	± .5	15
PDU-1016H-2	2	± .5	30
PDU-1016H-3	3	± 1.0	45
PDU-1016H-4	4	± 1.0	60
PDU-1016H-5	5	± 1.0	75
PDU-1016H-6	6	± 1.0	90
PDU-1016H-8	8	± 1.0	120
PDU-1016H-10	10	± 1.5	150
PDU-1016H-12	12	± 1.5	180
PDU-1016H-15	15	± 1.5	115
PDU-1016H-20	20	± 2.0	300
PDU-1016H-25	25	± 2.5	375
PDU-1016H-30	30	± 3.0	450
PDU-1016H-35	35	± 3.5	525
PDU-1016H-40	40	± 4.0	600
PDU-1016H-45	45	± 4.5	675
PDU-1016H-50	50	÷ 5.0	750
PDU-1016H-60	60	÷ 6.0	900
PDU-1016H-80	80	÷ 8.0	1,200
PDU-1016H-100	100	÷ 10.0	1,500

Digitally Programmable Delay Units

SERIES: PDU-1032H
(5-Bit) ECL Interfaced

data delay devices, inc. ®

Specifications:

- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ± 5% or 1 ns whichever is greater.
- **Inherent delay (T_{DO}):** 5.5 ns ± 1 ns for PDU-1032H-1 thru -5. Greater for rest of part numbers.
- **Propagation delay:**
  Address to output (T_{SUA}) = 3.6 ns typ.
  Enable to output (T_{SUE}) = 1.7 ns typ.
- **Power dissipation:** 615 mw typ.
- **Supply voltage:** −5 Vdc ± 5%.
- **Operating Temperature:** 0-70°C.
- **Temperature Coefficient:** 100 PPM/°C.
- **DC parameters:** See ECL-10KH Logic Table on Page 6.

Test Conditions

- **Input pulse-width:** ≥150% of Max. delay.
- **Input pulse spacing:** ≥3 times of Max. delay.
- **Input pulse voltage:** ECL logic.
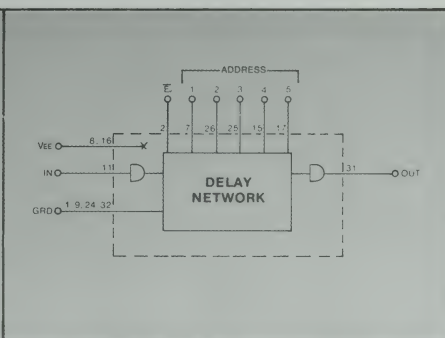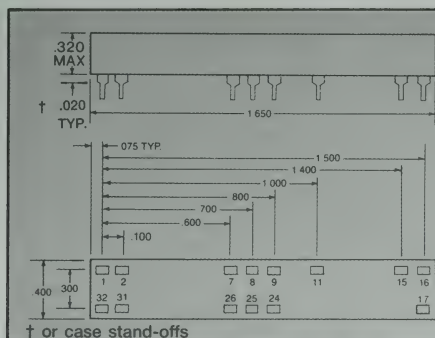- **Measurements taken @** T_a= 25°C, V_{EE}= −5V.

Features:

- Low propagation delay
- Input & output ECL buffered
- 5-BIT ECL programmable delay line
- Output same polarity of input
- Completely interfaced
- Compact & low profile

TRUTH TABLE

| Enable ($\overline{E_0}$)	Address					Delay Out
	5	4	3	2	1	
0	0	0	0	0	0	T_0
0	0	0	0	0	1	T_1
0	0	0	0	1	0	T_2
0	0	0	0	1	1	T_3
0	0	0	1	0	0	T_4
0	0	0	1	0	1	T_5
0	0	0	1	1	0	T_6
0	0	0	1	1	1	T_7
0	0	1	0	0	0	T_8
0	0	1	1	1	1	T_{15}
0	1	0	0	0	0	T_{16}
0	1	1	1	1	1	T_{31}
1	φ	φ	φ	φ	φ	0

0 = Logic 0   1 = Logic 1   φ = Don't care.
T_0 = Reference or inherent delay of unit.
$T_1 → T_{31}$ Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-1032H-0.5	0.5 ± 0.3	15.5
PDU-1032H-1	1 ± 0.5	31
PDU-1032H-2	2 ± 0.5	62
PDU-1032H-3	3 ± 1.0	93
PDU-1032H-4	4 ± 1.0	124
PDU-1032H-5	5 ± 1.0	155
PDU-1032H-6	6 ± 1.0	186
PDU-1032H-8	8 ± 1.0	248
PDU-1032H-10	10 ± 1.5	310
PDU-1032H-12	12 ± 1.5	371
PDU-1032H-15	15 ± 1.5	465
PDU-1032H-20	20 ± 2.0	620

Digitally Programmable Delay Units

SERIES: PDU-1064H
(6-Bit) ECL Interfaced

data delay devices, inc. ®
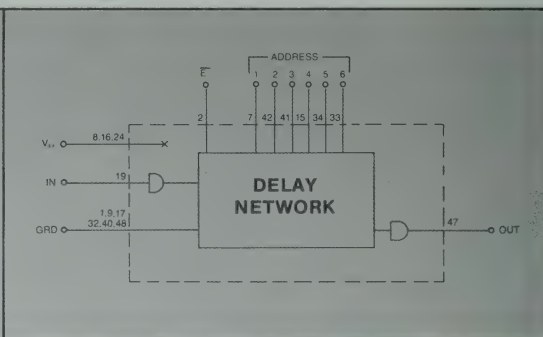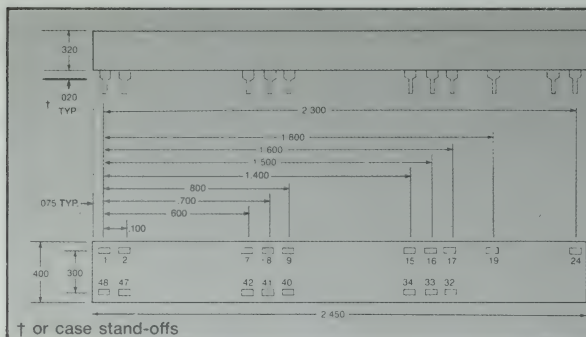

PDU-1064H
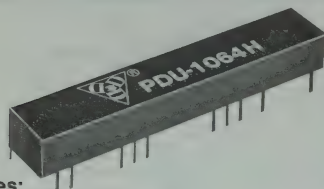
Features:

- Low propagation delay
- Input & output ECL buffered
- 6-BIT ECL programmable delay line
- Output same polarity of input
- Completely interfaced
- Compact & low profile

Specifications:

- Delay variation: Monotonic in one direction.
- Programmed delay tolerance: ± 5% or 2 ns whichever is greater.
- Inherent delay (T_{DO}): 12 ns typ.
- Propagation delay:
  Address to output (T_{SUA}) = 3.6 ns typ.
  Enable to output (T_{SUE}) = 1.7 ns typ.
- Power dissipation: 925 mw typ.
- Supply voltage: −5 Vdc ± 5%.
- Operating Temperature: 0-70°C.
- Temperature Coefficient: 100 PPM/°C.
- DC parameters: See ECL-10KH Logic Table on Page 6.

Test Conditions

- **Input pulse-width:**
  ≥150% of Max. delay.
- **Input pulse spacing:**
  ≥3 times of Max. delay.
- **Input pulse voltage:**
  ECL logic.
- **Measurements taken @**
  T_a= 25°C, V_{EE}= −5V.

† or case stand-offs

TRUTH TABLE

Enable ($\overline{E}_0$)	Address						Delay Out
	6	5	4	3	2	1	
0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	1	T_1
0	0	0	0	0	1	0	T_2
0	0	0	0	0	1	1	T_3
0	0	0	0	1	0	0	T_4
0	0	0	0	1	0	1	T_5
0	0	0	0	1	1	0	T_6
0	0	0	0	1	1	1	T_7
0	0	0	1	0	0	0	T_8
0	0	0	1	1	1	1	T_{15}
0	0	1	0	0	0	0	T_{16}
0	0	1	1	1	1	1	T_{31}
0	1	0	0	0	0	0	T_{32}
0	1	1	1	1	1	1	T_{63}
1	φ	φ	φ	φ	φ	φ	0

0 = Logic 0   1 = Logic 1   φ = Don't care.
T_0 = Reference or inherent delay of unit.
T_1 → T_{63} Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-1064H-0.5	0.5 ± 0.3	31.5
PDU-1064H-1	1 ± 0.5	63
PDU-1064H-2	2 ± 0.5	126
PDU-1064H-3	3 ± 1.0	189
PDU-1064H-4	4 ± 1.0	252
PDU-1064H-5	5 ± 1.0	315
PDU-1064H-6	6 ± 1.0	378
PDU-1064H-8	8 ± 1.0	504
PDU-1064H-10	10 ± 1.5	630

Digitally Programmable Delay Units

SERIES: PDU-1316
(4-Bit) TTL Interfaced
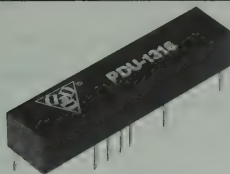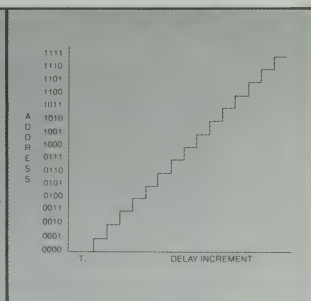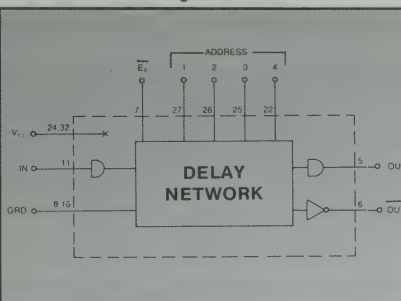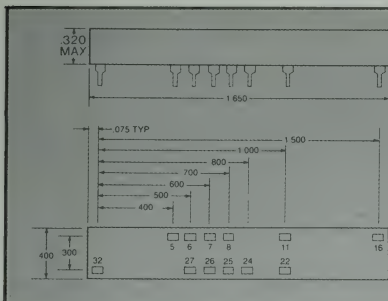
data delay devices, inc. ®

Features:

- Input & output TTL buffered
- 4-BIT TTL programmable delay line
- Two (2) separate outputs; inverting & non-inverting
- Completely interfaced
- Compact & low profile

Specifications:

- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ±5% or 1 ns whichever is greater.
- **Inherent delay (T$_{DO}$):**
  17 ns on pin 5 } typical
  15 ns on pin 6 } for PDU-1316-1 thru -10
  greater for rest of Part Numbers.
- **Propagation delay:**
  Address to output (T$_{SUA}$) = 12 ns typ.
  Enable to output (T$_{SUE}$) = 12 ns typ.
- **Power dissipation:** 740 mw max.
- **Supply voltage:** 5 Vdc ± 5%.
- **Operating temperature:** 0-70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **DC parameters:** See TTL-Standard Schottky Logic Table on Page 6.

Test Conditions:

- **Input pulse-width:**
  ≥ 150% of Max. delay.
- **Input pulse spacing:**
  ≥ 3 times of Max. delay.
- **Input pulse voltage:**
  TTL logic.
- **Measurements taken @**
  T$_a$ = 25°C; V$_{CC}$ = 5V.

TRUTH TABLE

Enable (E$_0$)	Address				Delay Out
	4	3	2	1	
0	0	0	0	0	T$_0$
0	0	0	0	1	T$_1$
0	0	0	1	0	T$_2$
0	0	0	1	1	T$_3$
0	0	1	0	0	T$_4$
0	0	1	0	1	T$_5$
0	0	1	1	0	T$_6$
0	0	1	1	1	T$_7$
0	1	0	0	0	T$_8$
0	1	0	0	1	T$_9$
0	1	0	1	0	T$_{10}$
0	1	0	1	1	T$_{11}$
0	1	1	0	0	T$_{12}$
0	1	1	0	1	T$_{13}$
0	1	1	1	0	T$_{14}$
0	1	1	1	1	T$_{15}$
1	Ø	Ø	Ø	Ø	0

0 = Logic 0   1 = Logic 1   Ø = Don't care.
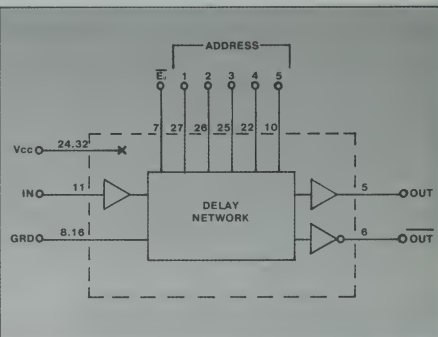T$_0$ = Reference or inherent delay of unit.
T$_1$ ⟶ T$_{15}$ = Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)		Total Programmed Delay (ns)
PDU-1316-.5	.5	.3	7.5
PDU-1316-1	1	.5	15.0
PDU-1316-2	2	.5	30.0
PDU-1316-3	3	1.0	45.0
PDU-1316-4	4	1.0	60.0
PDU-1316-5	5	1.0	75.0
PDU-1316-6	6	1.0	90.0
PDU-1316-8	8	1.0	120.0
PDU-1316-10	10	1.5	150.0
PDU-1316-12	12	1.5	180.0
PDU-1316-15	15	1.5	225.0
PDU-1316-20	20	2.0	300.0
PDU-1316-25	25	2.5	375.0
PDU-1316-30	30	3.0	450.0
PDU-1316-35	35	3.5	525.0
PDU-1316-40	40	4.0	600.0
PDU-1316-45	45	4.5	675.0
PDU-1316-50	50	5.0	750.0
PDU-1316-60	60	6.0	900.0
PDU-1316-80	80	8.0	1,200.0
PDU-1316-100	100	10.0	1,500.0

Digitally Programmable Delay Units

SERIES: PDU-1332
(5-Bit) TTL Interfaced
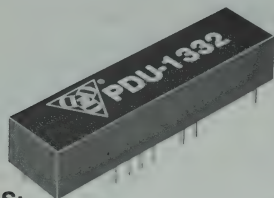
data delay devices, inc. ®

Specifications:

- **Propagation delay:**
  Address to output (T_{SUA}) = 12 ns typ.
  Enable to output (T_{SUE}) = 12 ns typ.
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ±5% or 1 ns whichever is greater.
- **Power dissipation:** 740 mw max.
- **Supply voltage:** 5 Vdc ± 5%.
- **Operating temperature:** 0-70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Inherent delay (T_{DO}):**
  17 ns on pin 5 } typical
  15 ns on pin 6 } for PDU-1332-1 thru -10
  greater for rest of Part Numbers.
- **DC parameters:** See TTL-Standard Schottky Logic Table on Page 6.

Test Conditions:

- **Input pulse-width:**
  > 150% of Max. delay.
- **Input pulse spacing:**
  > 3 times of Max. delay.
- **Input pulse voltage:**
  TTL logic.
- **Measurements taken**
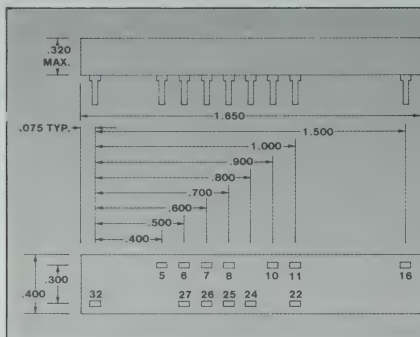 @ T_a = 25°C; V_{cc} = 5V.

FEATURES:

- Input & output TTL buffered
- 5-Bit TTL programmable delay line
- Two (2) separate outputs; inverting & non-inverting
- Completely interfaced
- Compact & low profile

TRUTH TABLE

Enable ($\overline{E_0}$)	Address					Delay Out
	5	4	3	2	1	
0	0	0	0	0	0	T_0
0	0	0	0	0	1	T_1
0	0	0	0	1	0	T_2
0	0	0	0	1	1	T_3
0	0	0	1	0	0	T_4
0	0	0	1	0	1	T_5
0	0	0	1	1	0	T_6
0	0	0	1	1	1	T_7
0	0	1	0	0	0	T_8
0	0	1	1	1	1	T_{15}
0	1	0	0	0	0	T_{16}
0	1	1	1	1	1	T_{31}
1	φ	φ	φ	φ	φ	0

0 = Logic 0   1 = Logic 1   φ = Don't care.
T_0 = Reference or inherent delay of unit.
$T_1 \rightarrow T_{31}$ Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-1332-0.5	0.5 ÷ 0.3	15.5
PDU-1332-1	1 ÷ 0.5	31
PDU-1332-2	2 ÷ 0.5	62
PDU-1332-3	3 ÷ 1.0	93
PDU-1332-4	4 ÷ 1.0	124
PDU-1332-5	5 ÷ 1.0	155
PDU-1332-6	6 ÷ 1.0	186
PDU-1332-8	8 ± 1.0	248
PDU-1332-10	10 ± 1.5	310
PDU-1332-12	12 ÷ 1.5	372
PDU-1332-15	15 ÷ 1.5	465
PDU-1332-20	20 ÷ 2.0	620

Digitally Programmable Delay Units

SERIES: PDU-1364
(6-Bit) TTL Interfaced

data delay devices, inc.

FEATURES:

- Input & output TTL buffered
- 6-Bit TTL programmable delay line
- Two (2) separate outputs; inverting & non-inverting
- Completely interfaced
- Compact & low profile

■ **Temperature Coefficient:** 100 PPM/°C.

Test Conditions:

- Input pulse-width: > 150% of Max. delay.
- Input pulse spacing: > 3 times of Max. delay.
- Input pulse voltage: TTL logic.
- Measurements taken @ $T_a = 25°C$; $V_{cc} = 5V$.

Specifications:

- **Propagation delay:**
  Address to output (T_{SUA}) 12 ns typ.
  Enable to output (T_{SUE}) 12 ns typ.
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ±5% or 1 ns whichever is greater.
- **Inherent delay (T_{DO}):**
  15 ns on pin 5 } typical
  13 ns on pin 6 } for PDU-1364-1 thru -5
  greater for rest of Part Numbers.
- **Power dissipation:** 950 mw max.
- **Supply voltage:** 5 Vdc ± 5%.
- **Operating temperature:** 0-70°C.
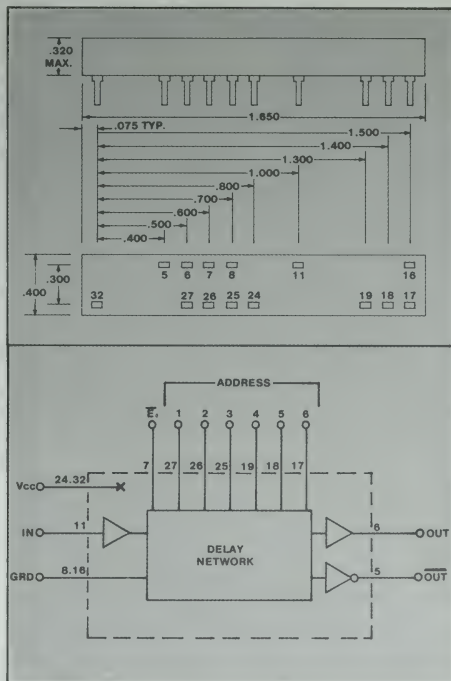- **DC parameters:** See TTL-Standard Schottky Logic Table on Page 6.

TRUTH TABLE

Enable (E)$_0$	Address						Delay Out
	6	5	4	3	2	1	
0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	1	T_1
0	0	0	0	0	1	0	T_2
0	0	0	0	0	1	1	T_3
0	0	0	0	1	0	0	T_4
0	0	0	0	1	0	1	T_5
0	0	0	0	1	1	0	T_6
0	0	0	0	1	1	1	T_7
0	0	0	1	0	0	0	T_8
0	0	0	1	1	1	1	T_{15}
0	0	1	0	0	0	0	T_{16}
0	0	1	1	1	1	1	T_{31}
0	1	0	0	0	0	0	T_{32}
0	1	1	1	1	1	1	T_{63}
1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1

0 = Logic 0   1 = Logic 1 ϕ = Don't care.
T_0 = Reference or inherent delay of unit.
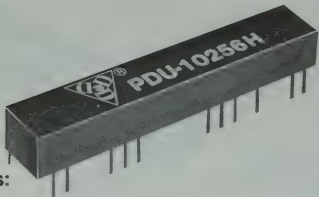T_1 T_{63} Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-1364-0.5	0.5 ÷ 0.3	31.5
PDU-1364-1	1 ÷ 0.5	63
PDU-1364-2	2 ÷ 0.5	126
PDU-1364-3	3 ÷ 1.0	189
PDU-1364-4	4 ÷ 1.0	252
PDU-1364-5	5 ÷ 1.0	315
PDU-1364-6	6 ÷ 1.0	378
PDU-1364-8	8 ÷ 1.0	504
PDU-1364-10	10 ± 1.5	630

Digitally Programmable Delay Units

SERIES: PDU-10256H
(8-Bit) ECL Interfaced
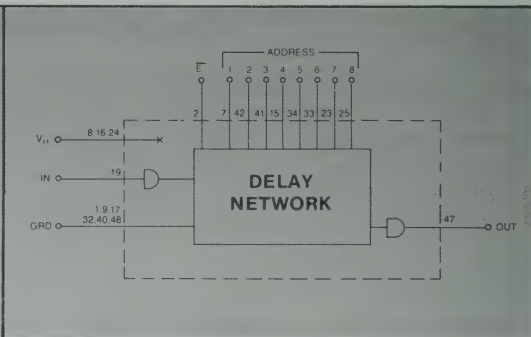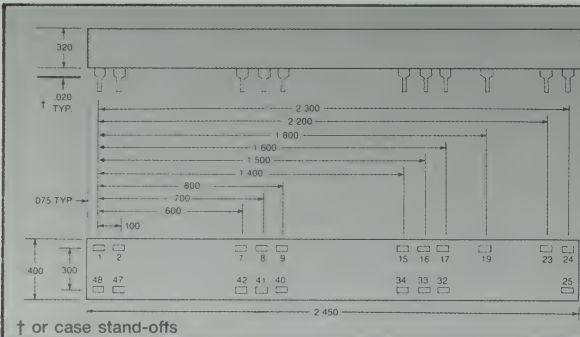
data delay devices, inc. ®

Features:

■ Low propagation delay
■ Input & output ECL buffered
■ 8-BIT ECL programmable delay line
■ Output same polarity of input
■ Completely interfaced
■ Compact & low profile

Specifications:

■ Delay variation: Monotonic in one direction.
■ Programmed delay tolerance: ± 5% or 1 ns whichever is greater.
■ Inherent delay (T$_{DO}$): 12 ns typ.
■ Propagation delay:
  Address to output (T$_{SUA}$) = 3.6 ns typ.
  Enable to output (T$_{SUE}$) = 1.7 ns typ.
■ Power dissipation: 925 mw typ.
■ Supply voltage: −5 Vdc ± 5%.
■ Operating Temperature: 0-70°C.
■ Temperature Coefficient: 100 PPM/°C.
■ DC parameters: See ECL-10KH Logic Table on Page 6.

Test Conditions

■ **Input pulse-width:**
  ≥150% of Max. delay.
■ **Input pulse spacing:**
  ≥3 times of Max. delay.
■ **Input pulse voltage:**
  ECL logic.
■ **Measurements taken @**
  Ta= 25°C, V$_{EE}$= −5V.

† or case stand-offs

TRUTH TABLE

Address (Bit No.)								Enable (E$_0$)	Delay Out
8	7	6	5	4	3	2	1		
0	0	0	0	0	0	0	0	0	T$_0$
0	0	0	0	0	0	0	1	0	T$_1$
0	0	0	0	0	0	1	0	0	T$_2$
0	0	0	0	0	0	1	1	0	T$_3$
0	0	0	0	0	1	0	0	0	T$_4$
0	0	0	0	0	1	1	1	0	T$_7$
0	0	0	0	1	0	0	0	0	T$_8$
0	0	0	0	1	1	1	1	0	T$_{15}$
0	0	0	1	0	0	0	0	0	T$_{16}$
0	0	0	1	1	1	1	1	0	T$_{31}$
0	0	1	0	0	0	0	0	0	T$_{32}$
0	0	1	1	1	1	1	1	0	T$_{63}$
0	1	0	0	0	0	0	0	0	T$_{64}$
0	1	1	1	1	1	1	1	0	T$_{127}$
1	0	0	0	0	0	0	0	0	T$_{128}$
1	1	1	1	1	1	1	1	0	T$_{255}$
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	0

0 = Logic 0   1 = Logic 1   Ø = Don't care.
T$_0$ = Reference or inherent delay of unit.
T$_1$ ⟶ T$_{255}$ multiplier of incremental delay

| Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-10256H-.5	.5 ± .3	127.5
PDU-10256H-1	1 ± .5	255
PDU-10256H-2	2 ± .5	510
PDU-10256H-3	3 ± 1.0	765
PDU-10256H-4	4 ± 1.0	1,020
PDU-10256H-5	5 ± 1.5	1,275
PDU-10256H-6	6 ± 1.5	1,530
PDU-10256H-7	7 ± 1.5	1,785
PDU-10256H-8	8 ± 2.0	2,040
PDU-10256H-9	9 ± 2.0	2,295
PDU-10256H-10	10 ± 2.0	2,550

NOTE: 1. For the sake of simplicity all 256 programmable steps are not shown in this truth table.
2. After Bit 6, the incremental delay tolerance is 5% of programmed delay.

Digitally Programmable Delay Units

SERIES: PDU-13256
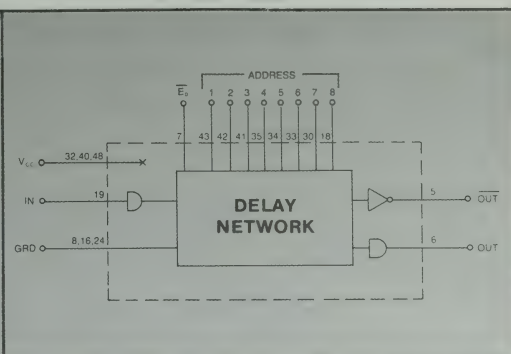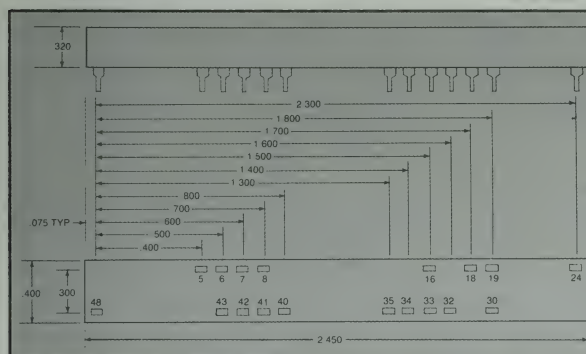**(8 Bit) TTL Interfaced**
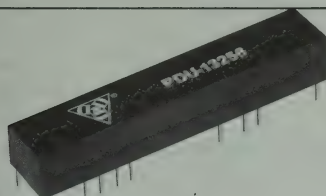
data delay devices, inc. ®

Specifications:
- Delay variation: Monotonic in one direction
- Programmed delay tolerance: ± 5% or 2 ns whichever is greater
- Inherent delay (T_{DO}): 19 ns on pin 6 } typical
  20 ns on pin 5 }
- Propagation delay:
  Address to output (T_{SUA}) — 12 ns typ.
  Enable to output (T_{SUE}) — 12 ns typ.
- Power dissipation: 1.1 w Max.
- Supply voltage: 5 Vdc ± 5%.
- Operating temperature: 0-70°C.
- Temperature Coefficient: 100 PPM/°C.
- DC parameters: See TTL-Standard Schottky Logic Table on Page 6.

Test Conditions
- Input pulse-width: ≥ 150% of Max. delay.
- Input pulse spacing: ≥ 3 times of Max. delay.
- Input pulse voltage: TTL logic.
- Measurements taken @ T_a = 25°C, V_{CC} = 5V.

Features:
- Input & output TTL buffered
- 8-BIT TTL programmable delay line
- Two (2) separate outputs; inverting & non-inverting.
- Completely interfaced
- Compact & low profile

TRUTH TABLE

Address (Bit No.)								Enable (E_0)	Delay Out
8	7	6	5	4	3	2	1		
0	0	0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	0	1	0	T_1
0	0	0	0	0	0	1	0	0	T_2
0	0	0	0	0	0	1	1	0	T_3
0	0	0	0	0	1	0	0	0	T_4
0	0	0	0	0	1	1	1	0	T_7
0	0	0	0	1	0	0	0	0	T_8
0	0	0	0	1	1	1	1	0	T_{15}
0	0	0	1	0	0	0	0	0	T_{16}
0	0	0	1	1	1	1	1	0	T_{31}
0	0	1	0	0	0	0	0	0	T_{32}
0	0	1	1	1	1	1	1	0	T_{63}
0	1	0	0	0	0	0	0	0	T_{64}
0	1	1	1	1	1	1	1	0	T_{127}
1	0	0	0	0	0	0	0	0	T_{128}
1	1	1	1	1	1	1	1	0	T_{255}
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	1

0 = Logic 0   1 = Logic 1   Ø = Don't care.
T_0 Reference or inherent delay of unit.
$T_1 \rightarrow T_{255}$ multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)		Total Programmed Delay (ns)
PDU-13256-.5	.5	- .3	127.5
PDU-13256-1	1	- .5	255
PDU-13256-2	2	- .5	510
PDU-13256-3	3	- 1.0	765
PDU-13256-4	4	- 1.0	1,020
PDU-13256-5	5	- 1.5	1,275
PDU-13256-6	6	- 1.5	1,530
PDU-13256-7	7	- 1.5	1,785
PDU-13256-8	8	- 2.0	2,040
PDU-13256-9	9	- 2.0	2,295
PDU-13256-10	10	- 2.0	2,550

NOTE: 1. For the sake of simplicity all 256 programmable steps are not shown in this truth table.
2. After Bit 6, the incremental delay tolerance is 5% of programmed delay.

Timing Definition for PPG-33F to PPG-38F
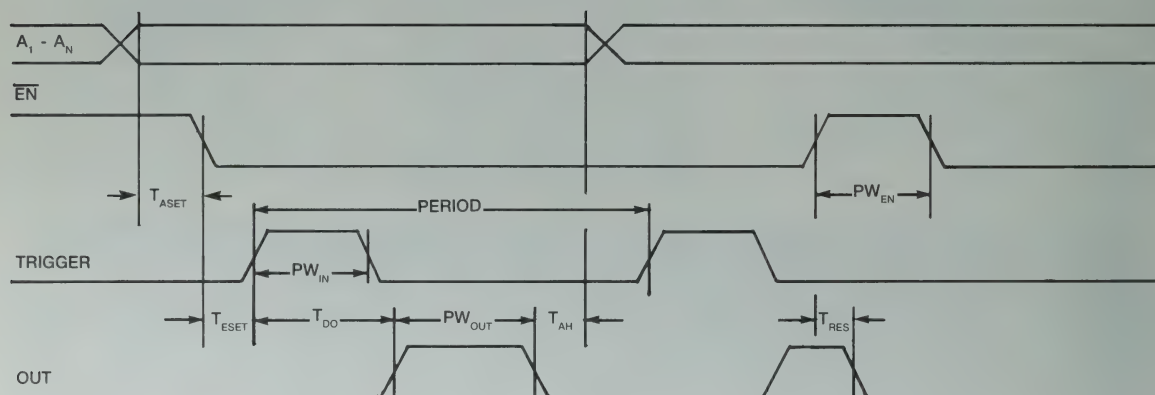
PW_{IN} =	Input pulse width.	(5 ns min.)
T_{DO} =	Inherent delay time.	
PW_O =	Inherent output pulse width.	
PW_{OUT} =	Output pulse width.	$(PW_P + PW_0)$
PW_P =	Programmed pulse width.	
PW_{EN} =	Enable pulse width high.	(10 ns min.)
PERIOD =	Input trigger period.	$(PW_{OUT} + 10$ ns min.)
T_{RES} =	Output pulse inhibit time.	(17 ns max.)
T_{ESET} =	Enable set time.	(9 ns min.)
T_{ASET} =	Address set time.	(0 ns min.)
T_{AH} =	Address hold time.	(0 ns min.)

Fast Logic

Programmable Pulse Generator

SERIES: PPG-33F
(3 Bit) TTL Interfaced

data delay devices, inc. ®

Features:
- Precise pulse widths
- 3-BIT address
- 1 ns to 50 ns incremental steps
- Trigger inherent delay (T_{DO}) — 4 ns typ.
- Inherent pulse width (PW_0) — 5 ns typ.
- Rising-edge triggered
- 14 pins DIP package
- Low profile
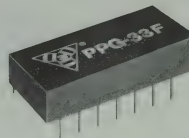
Specifications:
- Input pulse width: 6 ns min.
- Programmed pulse-width tolerance:
  $\pm$ 5% or 1 ns whichever is greater.
- Supply voltage (Vcc): 5 Vdc $\pm$ 5%.
- Operating temperature: 0° C to 70° C.
- Temperature coefficient: 100 PPM/° C.

- Supply current:
  I_{CCL}: 41 ma.
  I_{CCH}: 20 ma.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.
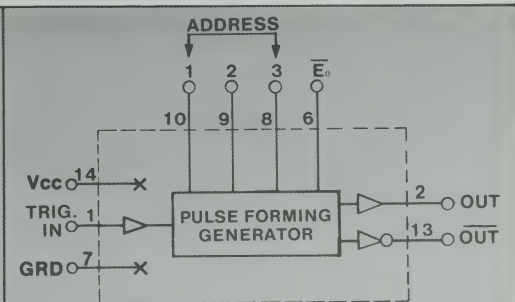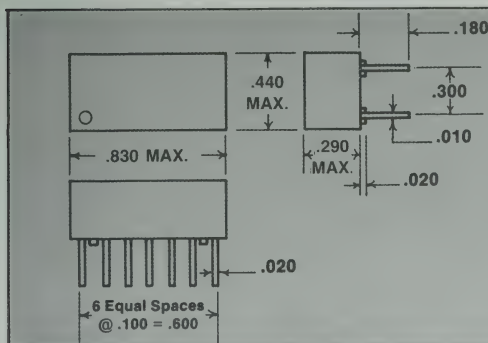
TRUTH TABLE

Enable ($\overline{E_0}$)	Address (Bit No.)			Pulse Width Out
	3	2	1	
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	ϕ	ϕ	ϕ	0

1 = High
0 = Low
ϕ = Don't care
T_0 = Reference or inherent pulse width.
T_1 to T_7 = Multiplier of pulse width.

Part Number	Incremental Pulse Width Per Step (ns)		Total Pulse Width Change (ns)
PPG-33F-.5	.5	$\pm$ .3	3.5
PPG-33F-1	1	– .4	7
PPG-33F-2	2	– .4	14
PPG-33F-3	3	– .5	21
PPG-33F-5	5	$\pm$ .6	35
PPG-33F-10	10	– 1.0	70
PPG-33F-15	15	– 1.3	105
PPG-33F-20	20	$\pm$ 1.5	140
PPG-33F-40	40	– 2.0	280
PPG-33F-50	50	$\pm$ 2.5	350

Contact us for specific requirements. We customize.

Fast Logic
Programmable Pulse Generator

SERIES: PPG-36F
**(6 Bit) TTL Interfaced**

data delay devices, inc. ®

Features:
- Precise pulse width.
- Inverted & non-inverted outputs.
- 6-BIT address.
- 1 ns to 10 ns incremental steps.
- Rising-edge triggered.
- 24 pins DIP package.
- Low profile.

Specifications:
- Trigger inherent delay (T_{DO}): 5 ns typ.
- Inherent pulse-width (PW_0): 14 ns typ.
- Pulse-width variation: monotonic in one direction.
- Programmed pulse-width tolerance: ± 5% or 1 ns whichever is greater.
- Supply voltage (Vcc): 5 Vdc ± 5%.
- Operating temperature: 0° C to 70° C.
- Temperature coefficient: 100 PPM/° C.
- Supply current:
  I_{CCL}: 72 ma.
  I_{CCH}: 27 ma.
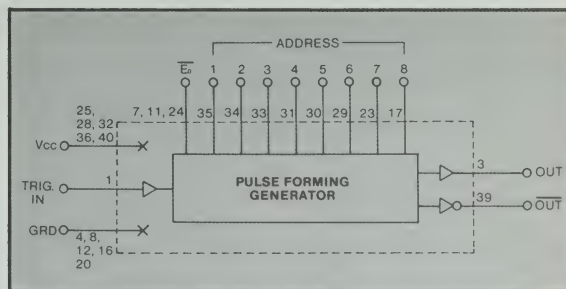- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.

TRUTH TABLE

Address (Bit No.)							
6	5	4	3	2	1	Enable ($\overline{E}_0$)	Pulse-Width Out
0	0	0	0	0	0	0	T_0
0	0	0	0	0	1	0	T_1
0	0	0	0	1	0	0	T_2
0	0	0	0	1	1	0	T_3
0	0	0	1	0	0	0	T_4
0	0	0	1	1	1	0	T_7
0	0	1	0	0	0	0	T_8
0	0	1	1	1	1	0	T_{15}
0	1	0	0	0	0	0	T_{16}
0	1	1	1	1	1	0	T_{31}
1	0	0	0	0	0	0	T_{32}
1	1	1	1	1	1	0	T_{63}
φ	φ	φ	φ	φ	φ	1	0

0 = Logic 0   1 = Logic 1   φ = Don't care.
T_0 = Reference or inherent pulse-width of unit.
$T_1 - T_{63}$ = Multiplier of incremental pulse-width.
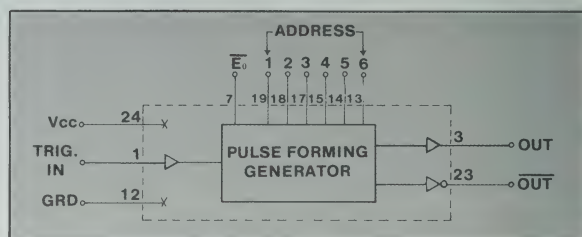
Part Number	Incremental Pulse-Width (ns)	Total Programmed Pulse-Width (ns)
PPG-36F-.5	.5 ± .3	31.5
PPG-36F-1	1 ± .5	63
PPG-36F-2	2 ± .5	126
PPG-36F-3	3 ± 1.0	189
PPG-36F-4	4 ± 1.0	252
PPG-36F-5	5 ± 1.5	315
PPG-36F-6	6 ± 1.5	378
PPG-36F-7	7 ± 1.5	441
PPG-36F-8	8 ± 2.0	504
PPG-36F-9	9 ± 2.0	567
PPG-36F-10	10 ± 2.0	630

Other customized units available.

Fast Logic
Programmable Pulse Generator

SERIES: PPG-38F
(8 Bit) TTL Interfaced

data delay devices, inc. ®

Features:
- Precise pulse width.
- Inverted & non-inverted outputs.
- 8 BIT address.
- .5 ns to 10 ns incremental steps.
- Rising-edge triggered.
- 40 pins DIP package.
- Low profile.

Specifications:
- **Trigger inherent delay:** 4 ns typ.
- **Inherent pulse-width:** 10 ns typ.
- **Pulse-width variation:** monotonic in one direction.
- **Programmed pulse-width tolerance:** $\pm$ 5% or 1 ns whichever is greater.
- **Supply voltage (Vcc):** 5 Vdc.
- **Operating temperature:** 0° C to 70° C.
- **Temperature coefficient:** 100 PPM/° C.
- **Supply current:**
  I_{CCL}: 150 ma.
  I_{CCH}: 42 ma.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

.580 MAX. .650 MAX. .280 MAX. 2.100 MAX .015 TYP. .100 TYP.
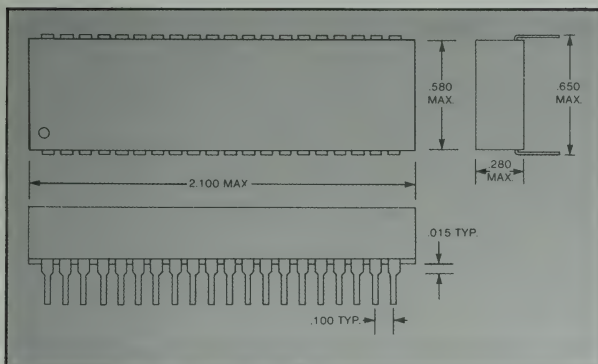
TRUTH TABLE

Address (Bit No.)								Enable ($\overline{E_0}$)	Pulse-Width Out
8	7	6	5	4	3	2	1		
0	0	0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	0	1	0	T_1
0	0	0	0	0	1	1	1	0	T_7
0	0	0	0	1	0	0	0	0	T_8
0	0	0	0	1	1	1	1	0	T_{15}
0	0	0	1	0	0	0	0	0	T_{16}
0	0	0	1	1	1	1	1	0	T_{31}
0	0	1	0	0	0	0	0	0	T_{32}
0	0	1	1	1	1	1	1	0	T_{63}
0	1	0	0	0	0	0	0	0	T_{64}
0	1	1	1	1	1	1	1	0	T_{127}
1	0	0	0	0	0	0	0	0	T_{128}
1	1	1	1	1	1	1	1	0	T_{255}
ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	0

0 = Logic 0   1 = Logic 1 ϕ = Don't care.
T_0 = Reference or inherent pulse-width of unit.
$T_1 \rightarrow T_{255}$ Multiplier of incremental pulse-width.

Part Number	Incremental Pulse-Width (ns)	Total Programmed Pulse-Width (ns)
PPG-38F-.5	.5 ÷ .3	127.5
PPG-38F-1	1 ÷ .5	255
PPG-38F-2	2 ÷ .5	510
PPG-38F-3	3 ÷ 1.0	765
PPG-38F-4	4 ÷ 1.0	1,020
PPG-38F-5	5 ÷ 1.5	1,275
PPG-38F-6	6 ÷ 1.5	1,530
PPG-38F-7	7 ÷ 1.5	1,785
PPG-38F-8	8 ÷ 2.0	2,040
PPG-38F-9	9 ÷ 2.0	2,295
PPG-38F-10	10 ÷ 2.0	2,550

Other customized units available.
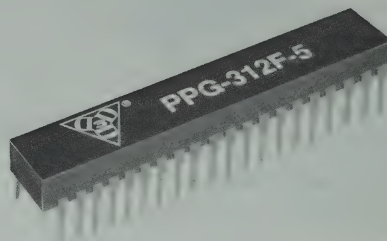
Programmable Pulse Generator

SERIES: PPG-312F
(12 Bit) TTL Interfaced

**data delay devices, inc.** ®

Features:

- ■ Precise pulse width.
- ■ Inverted & non-inverted outputs.
- ■ 12 BIT address.
- ■ .5 ns to 10 ns incremental steps.
- ■ Rising-edge triggered.
- ■ 40 pins DIP package.
- ■ Low profile.

Specifications:

- ■ **Trigger inherent delay:** 13 ns typ.
- ■ **Inherent pulse-width:** 19 ns typ.
- ■ **Pulse-width variation:** monotonic in one direction.
- ■ **Programmed pulse-width tolerance:** ± 2% or 2 ns whichever is greater.
- ■ **Supply voltage (Vcc):** 5 Vdc.
- ■ **Operating temperature:** 0˚ C to 70˚ C.
- ■ **Temperature coefficient:** 100 PPM/˚ C.
- ■ **Supply current:**
  Icc: 200 ma.
- ■ **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.
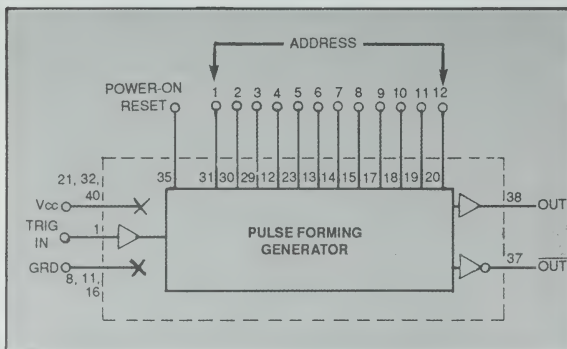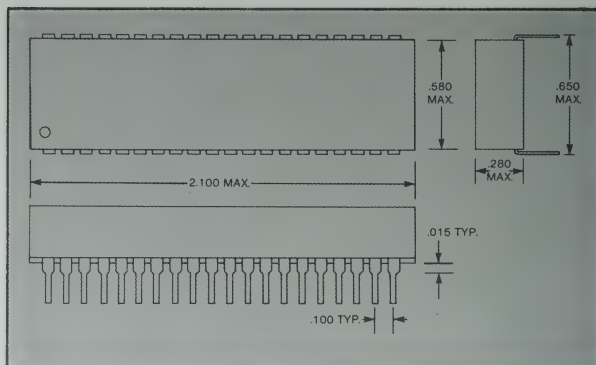
Part Number	Incremental Pulse-Width (ns)	Total Programmed Pulse-Width (μs)
PPG-312F-.5	.5 ± .3	2.048
PPG-312F-1	1 ± .5	4.096
PPG-312F-2	2 ± .5	8.192
PPG-312F-3	3 ± 1.0	12.288
PPG-312F-4	4 ± 1.0	16.384
PPG-312F-5	5 ± 1.5	20.480
PPG-312F-6	6 ± 1.5	24.576
PPG-312F-7	7 ± 1.5	28.672
PPG-312F-8	8 ± 2.0	32.768
PPG-312F-9	9 ± 2.0	36.864
PPG-312F-10	10 ± 2.0	40.960
PPG-312F-20	20 ± 2.0	81.920
PPG-312F-30	30 ± 2.0	122.880
PPG-312F-40	40 ± 2.0	163.840
PPG-312F-50	50 ± 2.5	204.800

Fast Logic
Variable Pulse Generator

Continuously Variable
T²L Interfaced

SERIES: VPG-40

data delay devices, inc. ®

Features:

- Input & output fully TTL interfaced and buffered.
- Low profile.
- Commercial & military type.
- Continuously adjustable.
- Multi-turn adjusting screw (40 turns approx.)
- Rising-edge trigger.

Specifications:

- Inherent pulse-width (PW_0): 15 ns typ.
- Trigger-inherent delay (TD_0): 6 ns typ.
- Pulse-width resolution: .12 ns.
- Output rise-time: 2 ns typ.
- Temperature coefficient: 100 PPM/°C.
- Temperature range: 0°C to 70°C standard. (−55°C to +125°C on request)*
- Supply voltage: 5.0 Vdc ± 5%.
- Power dissipation: 300 mw max.
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.

*Add "M" after Part No. Ex.: VPG-40-50M

Part No.	Min. Pulse-Width Variation (ns)
VPG-40-25	15
VPG-40-30	20
VPG-40-40	30
VPG-40-50	40
VPG-40-60	50
VPG-40-70	60
VPG-40-80	70
VPG-40-100	90
VPG-40-120	100
VPG-40-150	140
VPG-40-200	180

Other pulse-widths available on request.
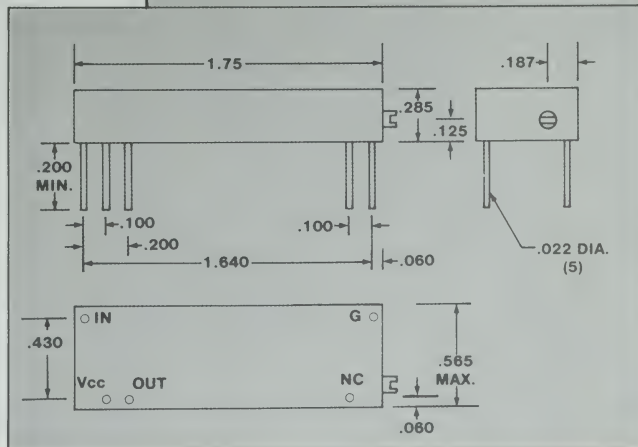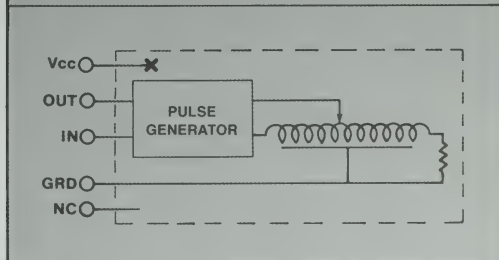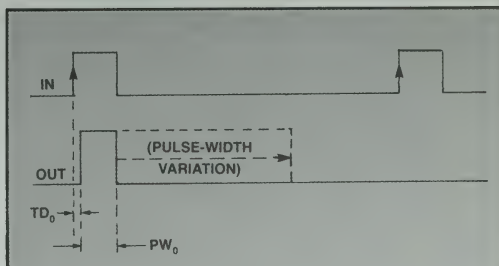
Pulse Width Controller
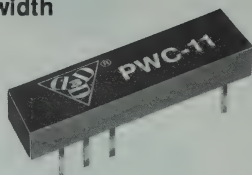
SERIES: PWC-11

ECL Interfaced
16 pins DIP

data delay devices, inc.

Features:

- ■ **Exact control of pulse width**
- ■ **Rising edge trigger**
- ■ **Auto-insertable**
- ■ **ECL input & outputs**
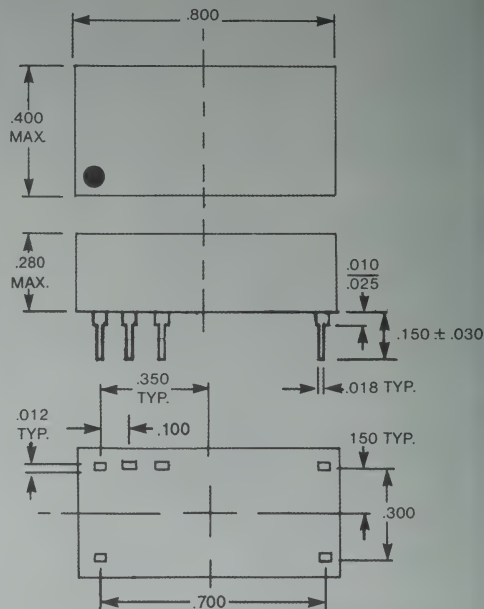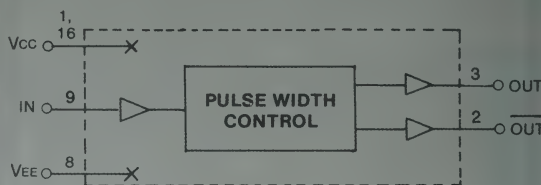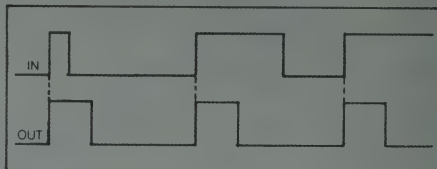- ■ **High speed**

Specifications:

- ■ **Input signal:** ECL.
- ■ **Minimum input pulse-width:** 10 ns.
- ■ **Output fan-out:** 70 ECL loads.
- ■ **Trigger inherent delay:** 5 ns typ.
- ■ **Pulse-width tolerance:** See table.
- ■ **Supply voltage:** −5.2 Vdc.
- ■ **Supply current:** 56 ma typ.
- ■ **Operating temperature:** −30°C to +85°C.
- ■ **Temperature coefficient:** 100 PPM/°C.
- ■ **Output rise-time:** 2 ns typ.
- ■ **DC Parameters:** See ECL-10KH Logic Table on Page 6.

Part No.	Pulse Width (in ns)	Maximum Pulse Rate (in Mhz)
PWC-11-5	5 ± 1	98
PWC-11-6	6 ± 1	80
PWC-11-7	7 ± 1	70
PWC-11-8	8 ± 1	60
PWC-11-9	9 ± 1	54
PWC-11-10	10 ± 1	49
PWC-11-15	15 ± 1	32
PWC-11-20	20 ± 1	24
PWC-11-25	25 ± 1	19
PWC-11-30	30 ± 1	15
PWC-11-35	35 ± 1.5	13
PWC-11-40	40 ± 1.5	11
PWC-11-45	45 ± 1.5	10
PWC-11-50	50 ± 1.5	9
PWC-11-60	60 ± 1.5	8
PWC-11-70	70 ± 2	7
PWC-11-75	75 ± 2	6
PWC-11-80	80 ± 2	6
PWC-11-90	90 ± 3	5
PWC-11-100	100 ± 3	4

====Fast Logic

Pulse Width Controller

SERIES: PWC-30

**TTL Interfaced
14 pin DIP**
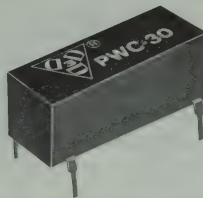
**data
delay
devices,** inc. ®

Features:

- **Exact control of pulse width**
- **Rising edge trigger**
- **Auto-insertable**
- **Low power consumption**
- **High speed**

Specifications:

- **Trigger Inherent Delay:** $T_{DO} = 6.5 \pm 1$ ns
  $\overline{T_{DO}} = 8.5 \pm 1$ ns
- **Pulse-width tolerance** = 5% or 2 ns
  (others on request)
- **Max. input PRR** = PW + 20 ns.
- **Supply voltage:** 5 Vdc.
- **Supply current:**
  I_{CCL}: 32 ma.
  I_{CCH}: 7 ma.
- **Operating temperature:** 0°C to 70°C
  (−55° to 125°C on request).*
- **Temperature coefficient:** 100 PPM/°C.
- **Output rise-time:** 2 ns typ.
- **DC parameters:** See TTL-Standard Schottky Logic
  Table on Page 6.
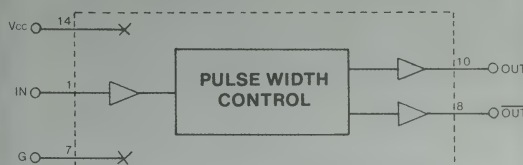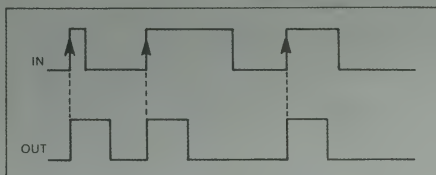
| Part No.	Pulse Width (ns)
PWC-30-5	5
PWC-30-10	10
PWC-30-15	15
PWC-30-20	20
PWC-30-30	30
PWC-30-40	40
PWC-30-50	50
PWC-30-60	60
PWC-30-75	75
PWC-30-100	100
PWC-30-125	125
PWC-30-150	150
PWC-30-175	175
PWC-30-200	200
PWC-30-250	250
PWC-30-300	300
PWC-30-350	350
PWC-30-400	400
PWC-30-500	500

====== Fast Logic

Pulse Width Controller

SERIES: PWC-32

TTL Interfaced
14 pin DIP

data delay devices, inc. ®

Features:

- ■ Two separate & equal pulse width controllers/package
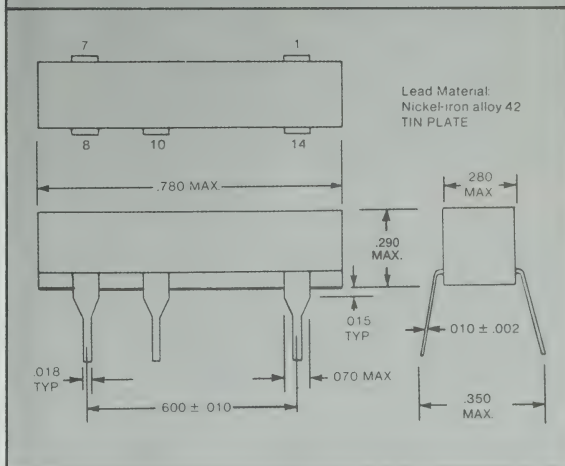- ■ Exact control of pulse width
- ■ Rising edge trigger
- ■ Auto-insertable
- ■ Low power consumption
- ■ High speed

Specifications:

- ■ Trigger inherent delay (T_{DO}) = 7 ns ± 1 ns.
  $(\overline{T_{DO}})$ = 9.5 ns ± 1 ns.
- ■ Pulse-width tolerance = 5% or 2 ns (others on request).
- ■ Max. input PRR = PW + 20 ns.
- ■ Supply voltage 5 Vdc ± 5%.
  I_{CCL}: 64 ma.
  I_{CCH}: 14 ma.
- ■ Operating temperature: 0°C to 70°C (−55° to 125°C on request).*
- ■ Temperature coefficient: 100 PPM/°C.
- ■ Output rise-time: 2 ns typ.
- ■ DC parameters: See TTL-Standard Schottky Logic Table on Page 6.

*DIL package used. E5 case.
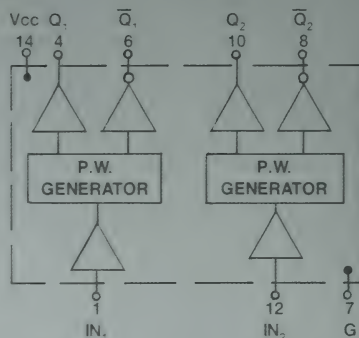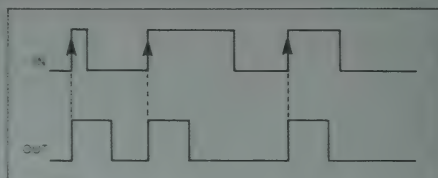
Part Number	Pulse Width (ns)
PWC-32-5	5
PWC-32-10	10
PWC-32-15	15
PWC-32-20	20
PWC-32-30	30
PWC-32-40	40
PWC-32-50	50
PWC-32-60	60
PWC-32-75	75
PWC-32-100	100
PWC-32-125	125
PWC-32-150	150
PWC-32-175	175
PWC-32-200	200
PWC-32-250	250

Other pulse-widths available on request.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.780 MAX

.290 MAX.

.280 MAX

.015 TYP

.010 ± .002

.018 TYP

.070 MAX

.600 ± .010

.350 MAX.
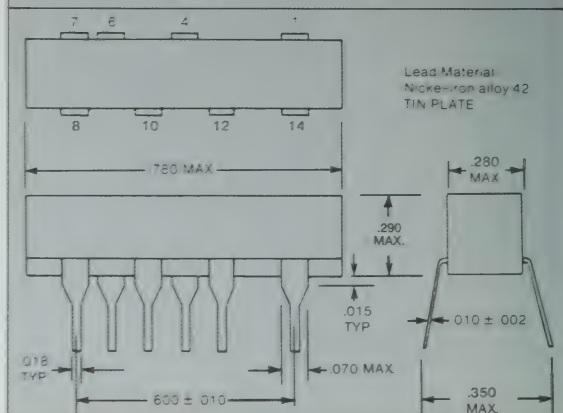
Programmable Pulse Discriminator

SERIES: PPD-23
(3 BIT) TTL Interfaced

data delay devices, inc.
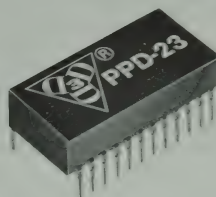
Features:

- **Discriminates against precisely programmed pulse widths.**
- **3-bit address.**
- **24 pins DIP.**
- **Low profile.**

Specifications:

- **Inherent pulse width (PW$_0$):** 5 ns typ.
- **Supply voltage:** 5 Vdc $\pm$ 5%.
- **Operating temperatures:** 0°C to 70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Power Dissipation:** 850 mw max.
- **DC parameters:** See TTL-Standard Schottky Logic Table on Page 6.
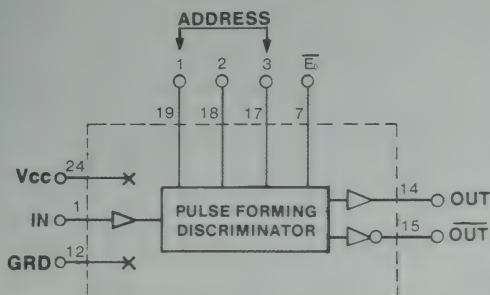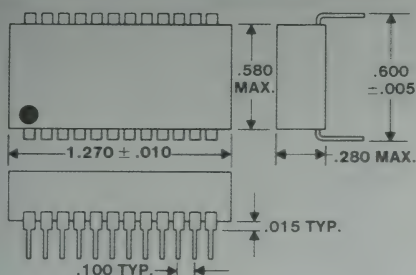
PW IN = Input pulse width
PW OUT = Output pulse = PW IN −4 ns
TP = Propagation delay = PW Programmed +6 ns

★CONDITION A: (PW IN ≤ PROGRAMMED PW.)

|← PW IN →|

IN
OUT
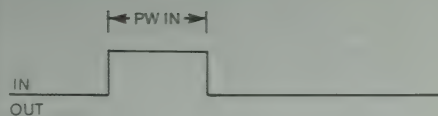
★ CONDITION B: (PW IN ≥ PROGRAMMED PW.)

|← PW IN →|

IN

OUT

|← TP →|← PW OUT →|
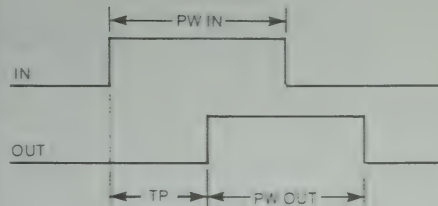
★See page vi for details timing.

ADDRESS

PULSE FORMING DISCRIMINATOR

Vcc ○24 ✕
IN ○1
GRD ○12 ✕

○14 OUT
○15 OUT

Part Number	Incremental Pulse Width Per Step (ns)	Total Programmed Pulse Width (ns)
PPD-23-1	1 − .4	7
PPD-23-2	2 ± .4	14
PPD-23-3	3 ± .5	21
PPD-23-5	5 ± .6	35
PPD-23-10	10 ± 1.0	70
PPD-23-15	15 ± 1.3	105
PPD-23-20	20 ± 1.5	140
PPD-23-40	40 ± 2.0	280
PPD-23-50	50 ± 2.5	350

Contact us for specific requirements. We customize.

Fast Logic
Programmable Pulse Discriminator
SERIES: PPD-56
(6 BIT) TTL Interfaced

data delay devices, inc. ®

Description:

The Programmable Discriminator Module, PPD-56 series, is a very powerful and versatile unit. It can be used to discriminate high pulse width or low pulse width or a limited range of pulse widths. It can be used as a programmable delay line with 7-Bit programmability. As an added feature it provides STATUS condition for selector A & B. By tying E_A & E_B to ground, the module becomes a programmable delay line and the delayed output signal is given by

$$A_{DELAYED} = 18 \text{ ns} + (A_0 - A_5)^* \text{ INCREMENT}$$

$$B_{DELAYED} = A_{DELAYED} + (B_0 \quad B_5)^* \text{ INCREMENT} + 9 \text{ ns}$$

Tying E_B to ground and E_A to positive level, the unit becomes a discriminator passing all pulse widths greater than programmed Selector A in accordance with the formula.

$$PW_{LOWER \text{ } LIMIT} = 8 \text{ ns} + (A_0 - A_5)^* \text{ INCREMENT}$$

Tying E_A to ground and E_B to positive level, the unit becomes a discriminator passing all pulse widths less than the programmed Selector B in accordance with the formula.

$$PW_{UPPER \text{ } LIMIT} = PW_{LOWER \text{ } LIMIT} + (B_0 - B_5)^* \text{ INCREMENT} + 3 \text{ ns}$$

Tying both E_A and E_B to positive level, the unit becomes a discriminator passing only a range of Pulse Widths defined by the equation:

$$PW_{RANGE} = PW_{UPPER \text{ } LIMIT} - PW_{LOWER \text{ } LIMIT}$$

Specifications:

- Discriminator input signal

  Minimum Pulse Width High (PW$_H$):   11 ns or $\frac{1}{8}$ of max. SELECT B, whichever is greater.

  Minimum Pulse Width Low (PW$_L$):   11 ns or (SELECT B–SELECT A) + 3 ns or $\frac{1}{8}$ of max. SELECT B, whichever is greater.

  Minimum Period = PW$_H$ + PW$_L$

- Programmable delay input signal

  Minimum Pulse Width High (PW$_H$):   8 ns or $\frac{1}{8}$ of max. SELECT B, whichever is greater.

  Minimum Period: $2 \times$ PW$_H$

- Supply voltage: 5 Vdc ± 5%
- Supply current:
  I_{CCL} = 80 ma typ.
  I_{CCH} = 190 ma typ.
- Operating temperature: 0°C to 70°C (–55°C to +125°C on request)*
- Temperature coefficient: 100 PPM/°C
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.

*Add "M" after P/N. Ex. PPD-56-5M

Part No.	Incremental Pulse-Width/ Delay (Selector A)(ns)	Total Programmed Pulse-Width/ Delay (Selector A)(ns)	Incremental Pulse-Width/ Delay (Selector B)(ns)	Total Programmed Pulse-Width/ Delay (Selector B)(ns)
PPD-56-.5	.5 ± .3	31.5	.5 ± .3	31.5
PPD-56-1	1 ± .5	63	1 ± .5	63
PPD-56-2	2 ± .5	126	2 ± .5	126
PPD-56-3	3 ± 1.0	189	3 ± 1.0	189
PPD-56-4	4 ± 1.0	252	4 ± 1.0	252
PPD-56-5	5 ± 1.5	315	5 ± 1.5	315
PPD-56-6	6 ± 1.5	376	6 ± 1.5	376
PPD-56-7	7 ± 1.5	441	7 ± 1.5	441
PPD-56-8	8 ± 2.0	504	8 ± 2.0	504
PPD-56-9	9 ± 2.0	567	9 ± 2.0	567
PPD-56-10	10 ± 2.0	630	10 ± 2.0	630
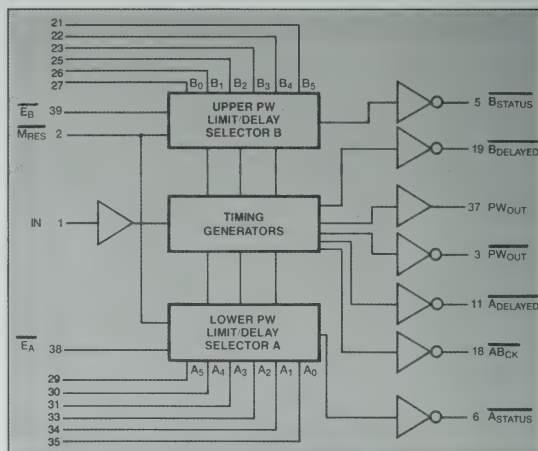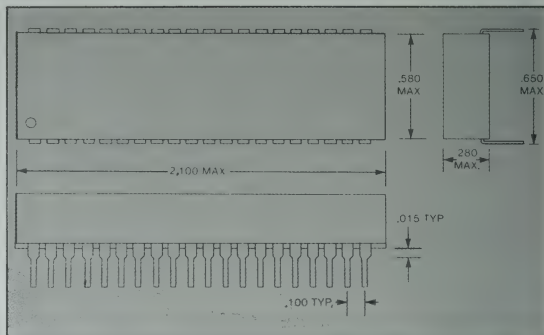
Vcc = 24, 28, 32, 36, 40   GRD = 4, 8, 12, 16, 20

Timing Waveform
(see other side)

Delay Function

IN

PW_i

T_{SU}

T_{SU}

$A_0 - A_5$

$B_0 - B_5$

T_A

$\overline{A}_{DELAYED}$

PW_0

T_B

$\overline{B}_{DELAYED}$

PW_0

$T_{SU} = \emptyset$ (min.)
$PW_i = PW_0$

$(A_0 - A_5) = \emptyset$ $T_A = 18$ ns
$(A_0 - A_5) \neq \emptyset$ $T_A = 18$ ns $+ (A_0 - A_5)^*$ INCREMENT

$A_0 - A_5$, $(B_0 - B_5) = \emptyset$ $T_B = 27$ ns
$(A_0 - A_5)$, $(B_0 - B_5) \neq \emptyset$ $T_B = 27$ ns $+ (A_0 - A_5)^*$ INCREMENT $+ (B_0 - B_5)^*$ INCREMENT
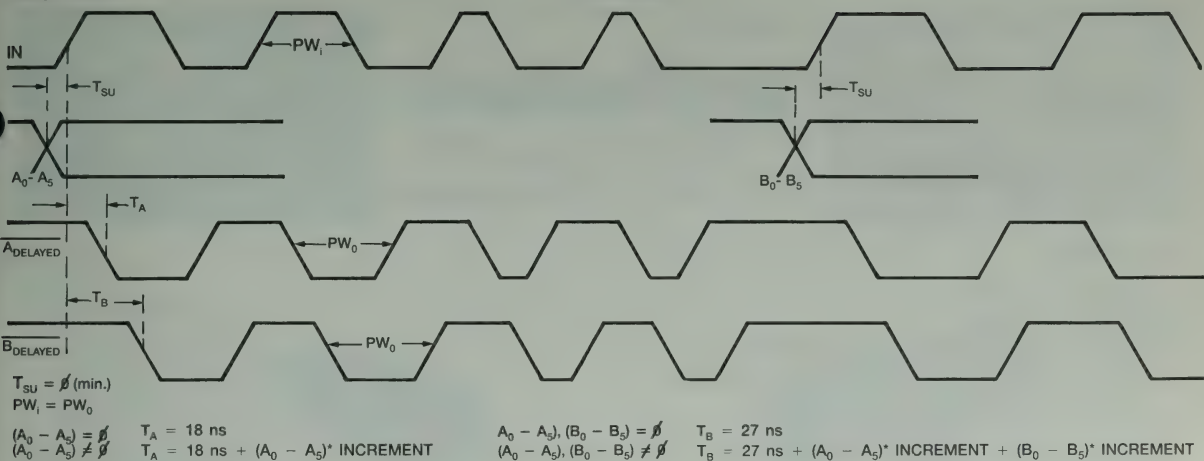
Discriminator Function

IN ① ② ③ ④ ⑤ ⑥

PW_i

$\overline{AB}_{CK}$

T_{SU} T_{SU}

$\overline{M}_{RES}$

T_{SU} T_{SU}

$\overline{E}_A$

$\overline{E}_B$ T_E

T_{SU} T_{SU}

T_{BHL} T_A T_A T_{BLH}

$\overline{A}_{STATUS}$

T_{CHL} T_A T_{CLH} T_A

$\overline{B}_{STATUS}$

T_D ① ③ ⑥

PW_OUT PW_0

$PW_i = PW_0$
$T_{SU} = \emptyset$

$T_A = 4$ ns typ. $T_{BHL} = 22$ ns
$T_E = 15$ ns min. $T_{BLH} = 21$ ns

$(A_0 - A_5) = \emptyset$ $T_{BHL} = 22 + (A_0 - A_5)^*$ INCREMENT
$(A_0 - A_5) \neq \emptyset$ $T_{BLH} = 21 + (A_0 - A_5)^*$ INCREMENT

$(A_0 - A_5)$, $(B_0 - B_5) = \emptyset$ $T_{CHL} = 30$ ns
  $T_{CLH} = 29$ ns

$(A_0 - A_5)$, $(B_0 - B_5) \neq \emptyset$ $T_{CHL} = 30 + [(A_0 - A_5) + (B_0 - B_5)]^*$ INCREMENT
  $T_{CLH} = 29 + [(A_0 - A_5) + (B_0 - B_5)]^*$INCREMENT

$(A_0 - A_5)$, $(B_0 - B_5) = \emptyset$ $T_D = 35$ ns
$(A_0 - A_5)$, $(B_0 - B_5) \neq \emptyset$ $T_D = 35 + [(A_0 - A_5) + (B_0 - B_5)]^*$ INCREMENT
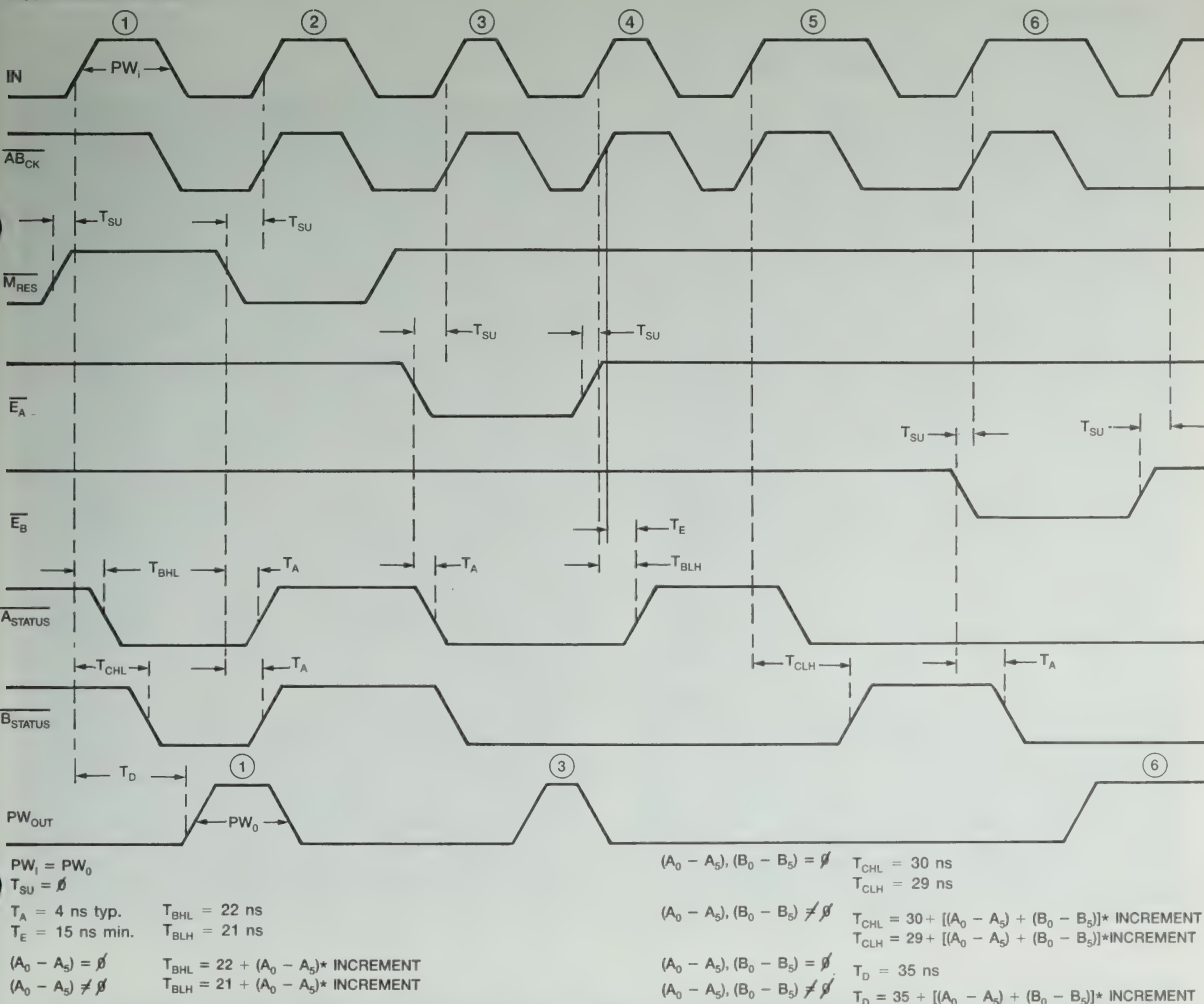
Fast Logic
Gated -Delay Line Oscillator
SERIES: DLO-31F

14 pins DIP
TTL Interfaced

data delay devices, inc.

Features:

- Auto-insertable.
- T^{2}L interfaced.
- Continuous or keyable wavetrain.
- Locked syncronization achieved with random gating signal.
- 14 pins DIP package.
- Low profile module.
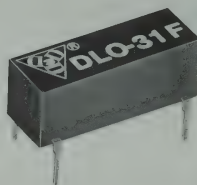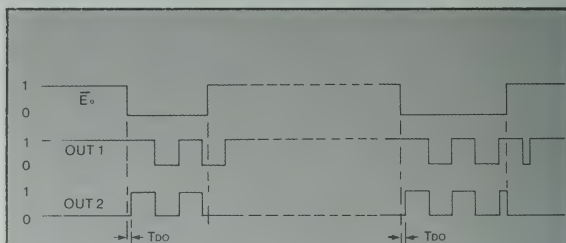- Available from 2 MHZ to 40 MHZ frequencies.

Specifications:

- Frequencies: See table; others on request.
- Tolerance: ± 2%.
- Temperature coefficient: 100 PPM/°C.
- Operating temperature: 0°-70°C.
- Supply voltage:5 Vdc ± 5%.
- Supply current: 40 ma.
- Storage temperature: −55°C to 125°C.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.
- Inherent delay (T$_{DO}$): 4 ns typ.
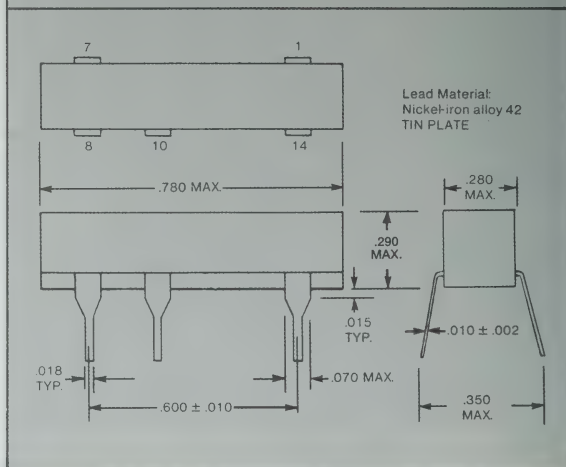
Part Number	Frequency	Part Number	Frequency
DLO-31F-2	2 MHz	DLO-31F-10	10 MHz
DLO-31F-2.5	2.5 MHz	DLO-31F-11	11 MHz
DLO-31F-3	3 MHz	DLO-31F-12	12 MHz
DLO-31F-3.5	3.5 MHz	DLO-31F-13	13 MHz
DLO-31F-4	4 MHz	DLO-31F-14	14 MHz
DLO-31F-4.5	4.5 MHz	DLO-31F-15	15 MHz
DLO-31F-5	5 MHz	DLO-31F-20	20 MHz
DLO-31F-5.5	5.5 MHz	DLO-31F-25	25 MHz
DLO-31F-6	6 MHz	DLO-31F-30	30 MHz
DLO-31F-7	7 MHz	DLO-31F-35	35 MHz
DLO-31F-8	8 MHz	DLO-31F-40	40 MHz
DLO-31F-9	9 MHz		

TRIGGER-RESPONSE

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.780 MAX.

.290 MAX.

.015 TYP.

.018 TYP.

.070 MAX.

.600 ± .010

.280 MAX.

.010 ± .002

.350 MAX.

Vcc 14
GRD 7
$\overline{E_0}$ 8

SQUARE WAVE OSCILLATOR

OUT 1 1
OUT 2 10
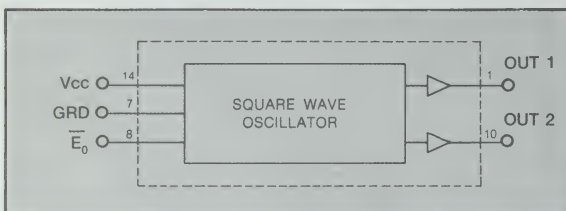
Fast Logic
Gated-Delay Line Oscillator
SERIES: DLO-32F

2-Phase
14 pins DIP
TTL Interfaced

data delay devices, inc.

Features:

- Auto-insertable.
- TTL interfaced.
- Continuous or keyable wavetrain.
- Locked syncronization achieved with random gating signal.
- 14 pins DIP package.
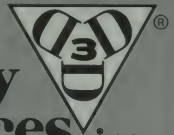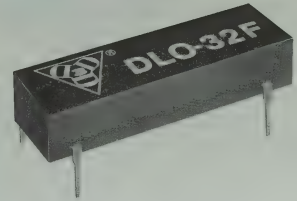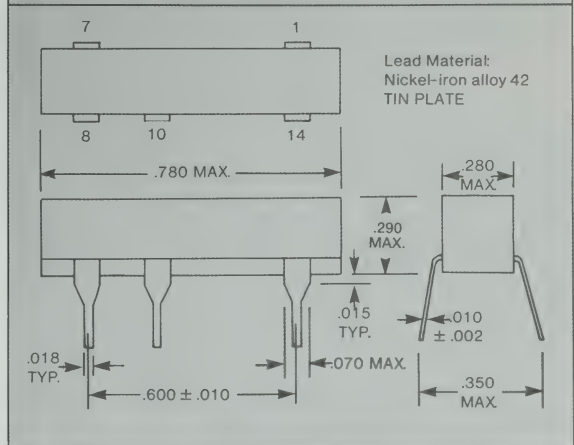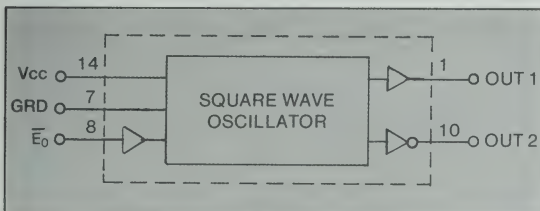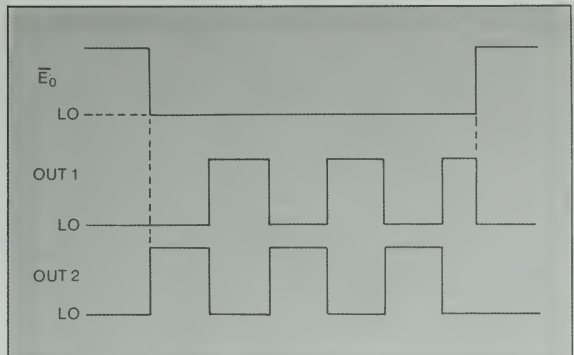- Low profile module.
- Available from 2 MHZ to 40 MHZ frequencies.
- Complimentary outputs.

Specifications:

- **Frequencies:** See table; others on request.
- **Tolerance:** ± 2%.
- **Temperature coefficient:** 100 PPM/°C.
- **Operating temperature:** 0°-70°C.
- **Supply voltage:** 5 Vdc ± 5%.
- **Supply current:** 40 ma. typ. (7 ma with $\overline{E}_0$ high).
- **Storage temperature:** −55°C to 125°C.
- **Inherent delay (T$_{DO}$):** 4 ns typ.
- **Pulse skewing** = 2.5 ns max.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Part Number	Frequency	Part Number	Frequency
DLO-32F-2	2 MHz	DLO-32F-10	10 MHz
DLO-32F-2.5	2.5 MHz	DLO-32F-11	11 MHz
DLO-32F-3	3 MHz	DLO-32F-12	12 MHz
DLO-32F-3.5	3.5 MHz	DLO-32F-13	13 MHz
DLO-32F-4	4 MHz	DLO-32F-14	14 MHz
DLO-32F-4.5	4.5 MHz	DLO-32F-15	15 MHz
DLO-32F-5	5 MHz	DLO-32F-20	20 MHz
DLO-32F-5.5	5.5 MHz	DLO-32F-25	25 MHz
DLO-32F-6	6 MHz	DLO-32F-30	30 MHz
DLO-32F-7	7 MHz	DLO-32F-35	35 MHz
DLO-32F-8	8 MHz	DLO-32F-40	40 MHz
DLO-32F-9	9 MHz		

Lead Material: Nickel-iron alloy 42 TIN PLATE

.780 MAX.
.280 MAX.
.290 MAX.
.015 TYP.
.010 ± .002
.018 TYP.
.070 MAX.
.600 ± .010
.350 MAX.

Vcc — 14
GRD — 7
$\overline{E}_0$ — 8

SQUARE WAVE OSCILLATOR

1 — OUT 1
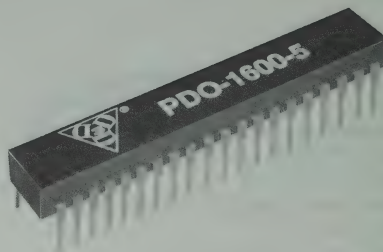10 — OUT 2

16 BIT Programmable Gated-Oscillator

SERIES: PDO-1600

data delay devices, inc. ®

FEATURES:

- Completely TTL interfaced and buffered.
- Enable pin provided.
- Microprocessor or computer controlled.
- VCO replacement.
- Reliable and repeatable frequency generation.
- Very stable frequency.
- Jitter-free

Specifications:

- **Period variation:** monotonic in one direction.
- **Duty cycle:** 50%.
- **Period tolerance:** ±5%.
- **Inherent period** = period increment.
- **Power dissipation:** 1.1 W max.
- **Supply voltage:** 4.75 to 5.25 Vdc.
- **Operating temperature:** 0-70° C.
- **Temperature coefficient:** 100 PPM/° C.
- **Inherent delay (T_{DO}) =** 12 ns.
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Part Number	Incremental Period (ns)	Upper Frequency (Mhz)
PDO-1600-5	100	5.0
PDO-1600-10	50	10.0

ADDRESS (BIT NO.)

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

32 5 6 7 9 10 11 12 23 13 14 15 17 18 19 20

$\overline{E_0}$ ○ ── 34

Square Wave Oscillator

4, 8, 16

GRD ○

Vcc ○ ── 21, 40

3 ── ○ OUT

$\overline{E_0}$

1
0

OUT

1
0

T_{DO} T_{DO}

TRIGGER-RESPONSE
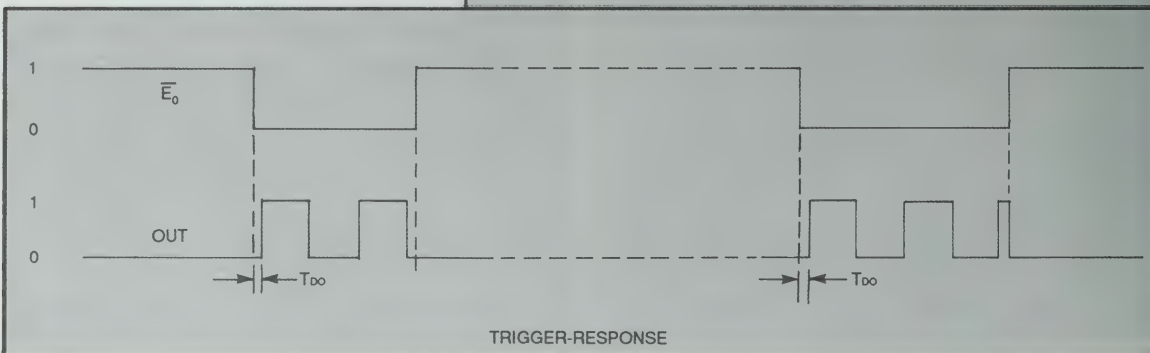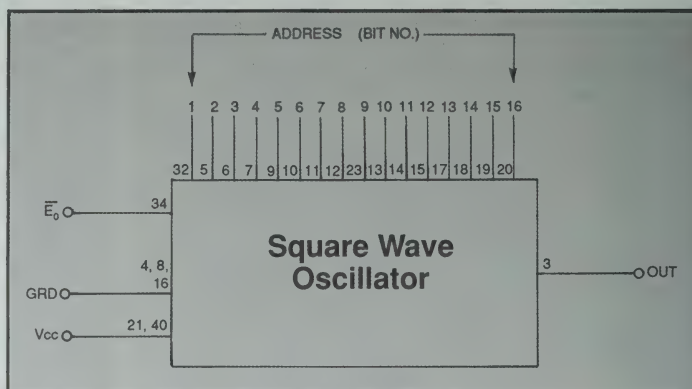
FAST
Dynamic Memory Timer
TTL Interfaced
14 pins DIP
SERIES: DMT-300

data delay devices, inc.

Features:
- All DRAM's timing generated from a single MREQ signal
- Accurate and stable timing
- Rising-edge triggered
- PC board economy
- Saves components
- Low profile

Specifications:
- Input pulse width: 4 ns min.
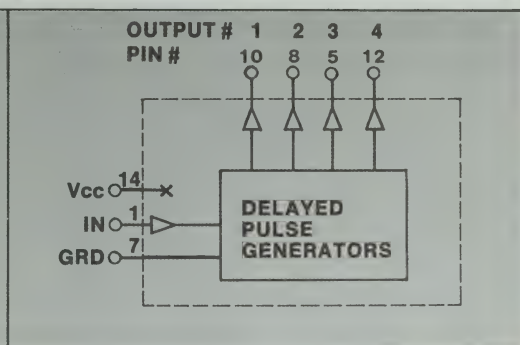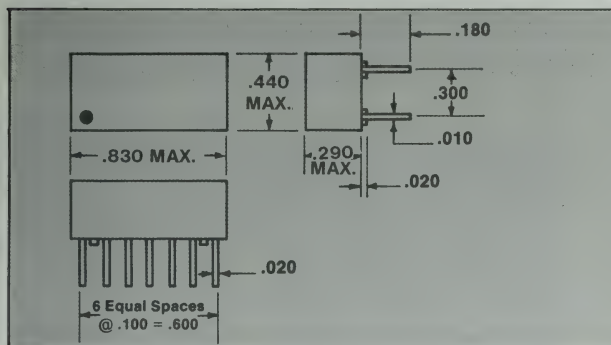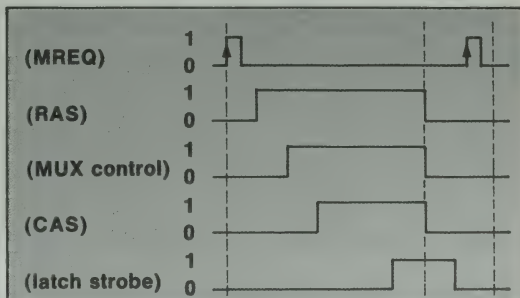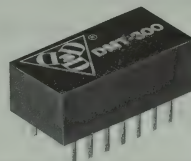- Max. rep. rate of (MREQ) = T_E of latch strobe.
- Time delay tolerance: ±5% or 2 ns whichever is greater.
- Supply voltage (Vcc): 5 Vdc ± 5%.
- Operating temperature: 0° C to 70° C.
- Temperature coefficient: 100 PPM/°C.
- Power dissipation: 740 mw max.
- DC parameters: See TTL-Standard Schottky Logic Table on Page 6.

OUTPUT # 1 2 3 4
PIN #   10 8 5 12

Vcc 14
IN 1
GRD 7

DELAYED PULSE GENERATORS

Part No.	Output 1 (RAS)		Output 2 (MUX CONTROL)		Output 3 (CAS)		Output 4 (Latch Strobe)	
	LE	TE	LE	TE	LE	TE	LE	TE
DMT-301-1	15	190	40	190	65	190	140	190
DMT-301-2	15	165	40	165	65	165	115	215
DMT-301-3	15	190	40	190	65	190	190	240
DMT-301-4	15	215	40	215	65	215	165	265
DMT-301-5	15	265	40	265	115	265	215	315
DMT-301-6	15	215	40	215	65	215	165	335
DMT-301-7	15	165	30	165	50	165	115	265
DMT-301-8	15	135	30	135	50	135	85	235
DMT-301-9	15	275	40	275	65	275	220	370
DMT-301-10	15	120	40	120	65	120	115	215
DMT-301-11	15	185	40	185	65	185	125	185
DMT-301-12	10	90	20	90	40	90	100	120
DMT-302-1	15	265	65	265	90	265	215	315
DMT-302-2	15	290	65	290	115	290	240	340
DMT-302-3	15	315	65	315	140	315	265	365
DMT-303-1	25	300	75	300	125	300	250	350

1. All timing above in ns.
2. Many more customized designs available upon request.

Manchester Decoder
SERIES: MAD-85

**14 pins DIP
TTL Interfaced**

data delay devices, inc.

Features:
- TTL input & outputs.
- 14 pins DIP.
- Data Rates to 25 MB/S.
- Self Syncronizing within one BIT time.

Application:
- Local Area Network (LAN) interfaces.
- Ethernet Bus interfaces.
- IEEE 802 LAN interfaces.
- Fiber optic data links.
- Multidrop Bus interfaces.

Specifications:
- Operating temperature: 0° to 70°C.
- Temperature coefficient: 100 PPM/°C.
- Supply voltage V_{cc}: 5 Vdc ± 5%.
- Power dissipation: 740 mw max.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.
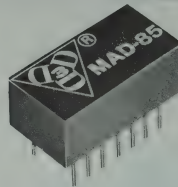
Part No.	Operating Data Rates	Part No.	Operating Data Rates
MAD-85-1	1 MB/S	MAD-85-14	14 MB/S
MAD-85-2	2 MB/S	MAD-85-15	15 MB/S
MAD-85-3	3 MB/S	MAD-85-16	16 MB/S
MAD-85-4	4 MB/S	MAD-85-17	17 MB/S
MAD-85-5	5 MB/S	MAD-85-18	18 MB/S
MAD-85-6	6 MB/S	MAD-85-19	19 MB/S
MAD-85-7	7 MB/S	MAD-85-20	20 MB/S
MAD-85-8	8 MB/S	MAD-85-21	21 MB/S
MAD-85-9	9 MB/S	MAD-85-22	22 MB/S
MAD-85-10	10 MB/S	MAD-85-23	23 MB/S
MAD-85-11	11 MB/S	MAD-85-24	24 MB/S
MAD-85-12	12 MB/S	MAD-85-25	25 MB/S
MAD-85-13	13 MB/S		

.180
.440 MAX.
.300
.830 MAX.
.290 MAX.
.010
.020
.020
6 Equal Spaces @ .100 = .600

V_{cc} 14
CODE IN 1
G 7
DECODER
8 $\overline{DATA}$
4 $\overline{CLK}$

MANCHESTER CELL

N 1 | N + 1 0 | N + 2 0 | N + 3 0 | N + 4 1 | N + 5 0

Rx T_{BIT}

DATA OUT/ .75 T_{BIT}
1.25 T_{BIT}

CK/

DATA BIT/ 0 N | 1 N + 1 | 1 N + 2 | 1 N + 3 | 0 N + 4

$T_{BIT} = {}^1/_{BAUD\ RATE}$

NOTE: Manchester Coding Scheme
1. Transition in center of bit-time of Manchester code.
2. Logic 0 is coded as a 1 to 0 center cell transition.
3. Logic 1 is coded as a 0 to 1 center cell transition.

Manchester Encoder
SERIES: MAE-86

14 pins DIP
TTL Interfaced

data delay devices, inc. ®

Features:

- T²L input & outputs.
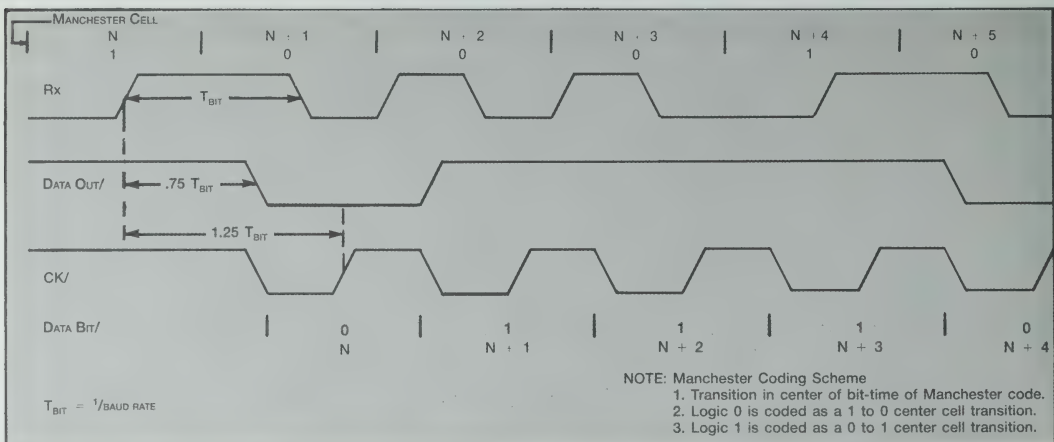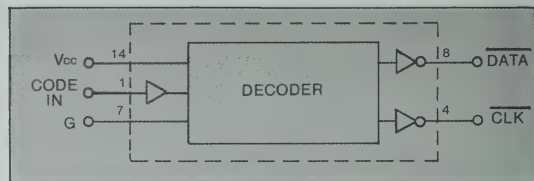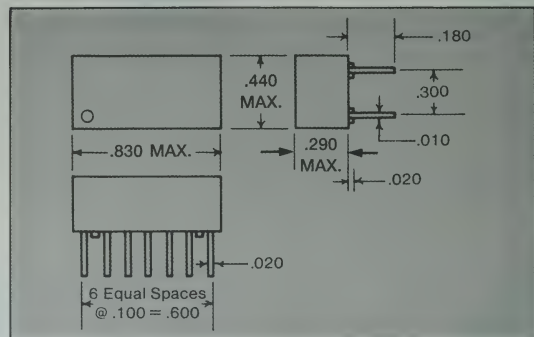- 14 pins DIP.
- Data rates to 30 MB/S.

Application:

- Local Area Network (LAN) interfaces.
- Ethernet Bus interfaces.
- IEEE 802 LAN interfaces.
- Fiber optic data links.
- Multidrop Bus interfaces.

Specifications:

- **Operating temperature:** 0° to 70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Supply voltage** V_{cc}**:** 5 Vdc ± 5%.
- **Power dissipation:** 300 mw max.
- **CLK$_{IN}$** = 1 × operating data rates
- **CLK$_{IN}$** duty cycle = 50%
- **DC parameters:** See TTL-Standard Schottky Logic Table on Page 6.
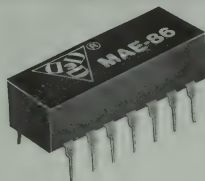
Description:

An innovating design approach has been used in this Manchester Encoder to reduce the system clock frequency by ½. The reduction in system clock eliminates many high frequency problems in PC board lay-out and cross-talk.

Most commercially available Manchester Encoders require an input clock frequency (CLK IN) of twice the operating data rates. In the MAE-86 Manchester Encoder the (CLK IN) input clock is equal to the operating data rates.

One single unit covers the complete range of operating data rate up to 25 MB/S. Its low profile, standard 14 pins DIP package and low power consumption makes it completely compatible with Schottky TTL circuitry.

Lead Material
Nickel-iron alloy 42
TIN PLATE

NOTE: Manchester Coding Scheme
1. Transition in center of bit-time of Manchester code.
2. Logic 0 is coded as a 1 to 0 center cell transition.
3. Logic 1 is coded as a 0 to 1 center cell transition.

T_S 0 min.
T_H 7 ns typ. T_{DATA} = 1 CK period + 23 ns max.
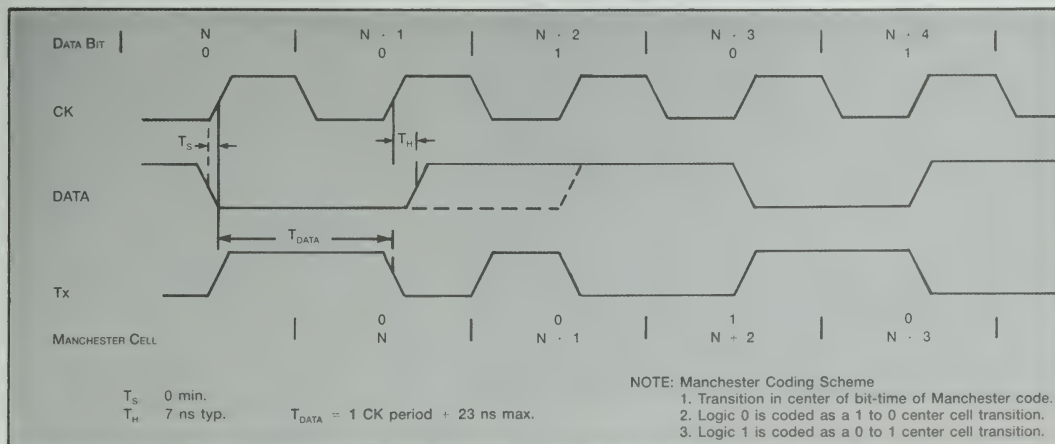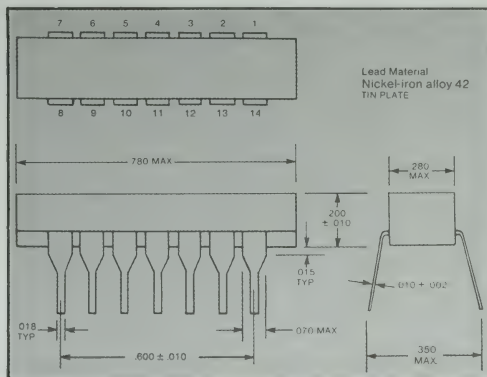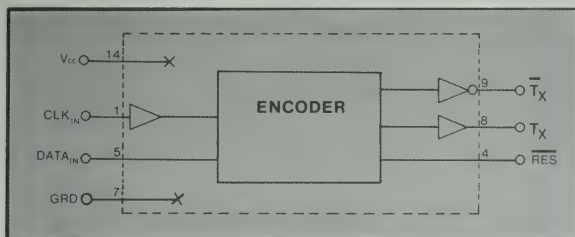
1553 Manchester Encoder
SERIES: MAE-8782   (20 MBAUD)

data delay devices, inc.

Specifications:

- **Completely TTL buffered.**
- **Operating temperature:** 0°C to 70°C (-55°C to +125°C on request).
- **Temperature coefficient:** 100 PPM/°C.
- **Supply voltage:** 5 Vdc ± 5%.
- **Power dissipation:** 1.3 w typ.
- **Data rate:** 20 MBIT/sec (others on request).
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.

MAE-8782

Vcc — 24

DATA IN — 1

MAE-8782

14 — SHIFT CK

SEND — 5

GRD — 12

23 — 1553 MANCHESTER DATA OUT

See Other Side For Timing Waveform

24   13

1   12

.580 MAX.

.600 ±.005

← 1.270 ± .010 →

.280 MAX.

.015 TYP.

.100 TYP.→

MAE-8782 Timing Waveforms

SEND

SHIFT CK

DATA IN

Tx

Tx

$PW_{SEND\ H} = 70$ nsec min.

$PW_{SEND\ L} = 2 \cdot PW_{SYNC} + 16 \cdot PW_{DAT\ Ø}$

$T_{CK} = P_{CK} = 75$ nsec typ.

$P_{CK}\ Ø = 50$ nsec $\pm 5\%$.

$PW_{SYNC} = 75$ nsec $\pm 5\%$.

$PW_{DAT}\ Ø = 50$ nsec $\pm 5\%$.

$PW_1 = 25$ nsec $\pm 5\%$.

$T_D\ Ø = 5$ nsec typ.

** Data Delay Devices Rising Edge Triggered
Pulse Width Controller. It generates a
precise and stable 75 nsec pulse.
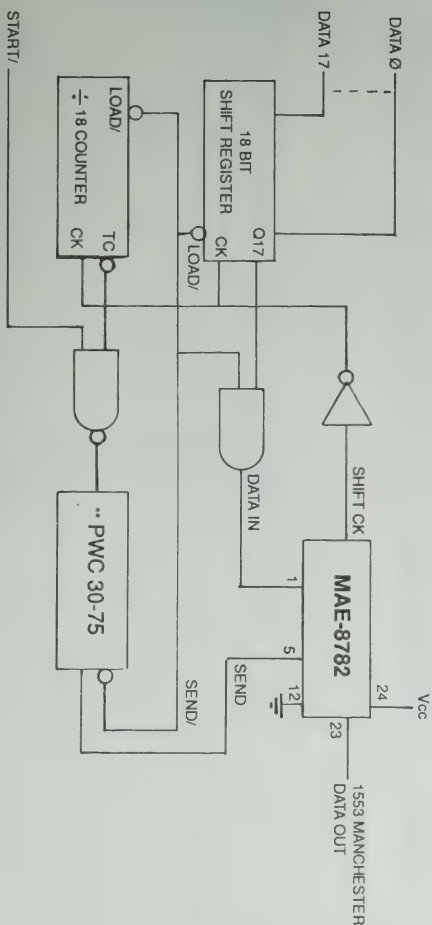
Typical Encoder Interface
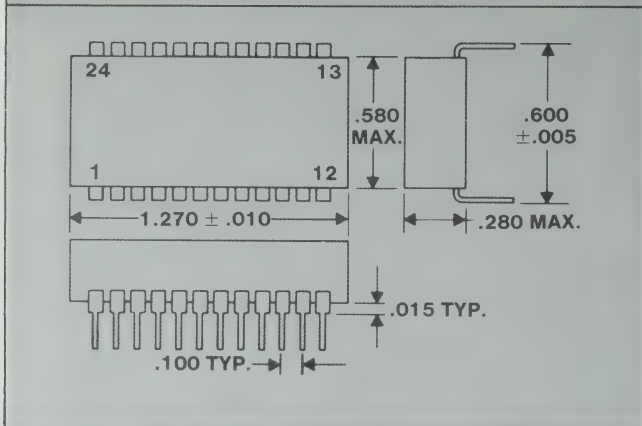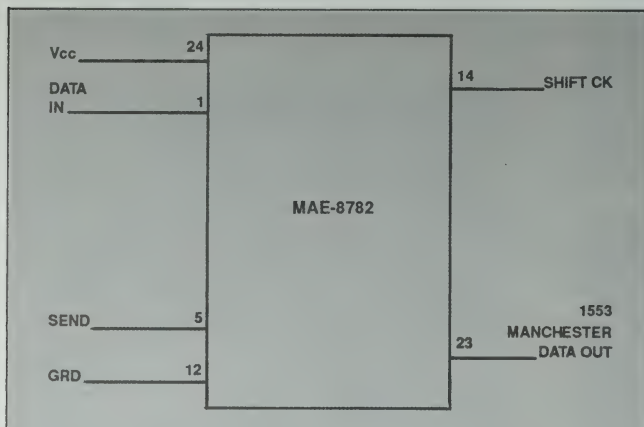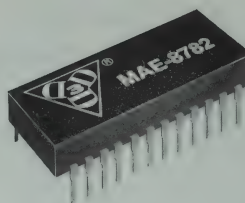
1553 Manchester Decoder

SERIES: MAD-8783 (20 MBAUD)
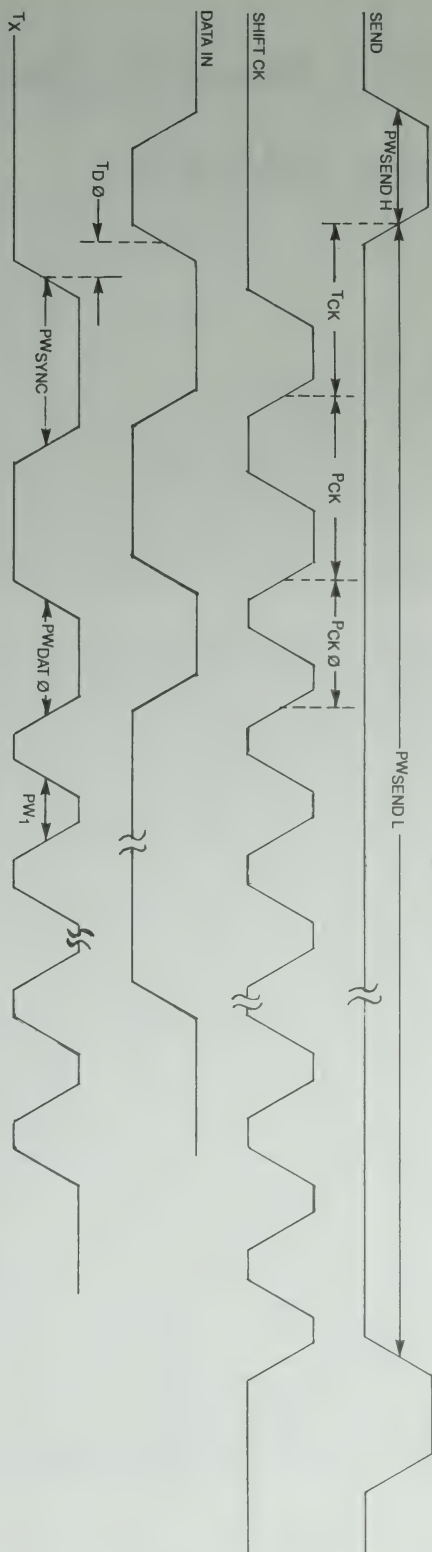
data delay devices, inc. ®

Specifications:

- **Completely TTL buffered.**
- **Operating temperature:** 0°C to 70°C (-55°C to +125°C on request).
- **Temperature coefficient:** 100 PPM/°C.
- **Supply voltage:** 5 Vdc ± 5%.
- **Power dissipation:** 500 mw typ.
- **Data rate:** 20 MBIT/sec (others on request).
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.

MAD-8783

Vcc ___ 24

1553 MANCHESTER DATA IN ___ 1

MAD-8783

13 ___ DATA OUT

18 ___ CK/

RES/ ___ 10

GRD ___ 12

11 ___ SYNC FLAG

See Other Side For Timing Waveform

24   13

1   12

.580 MAX.

.600 ±.005

◄──── 1.270 ± .010 ────►

◄──►┤ .280 MAX.

.015 TYP.

.100 TYP. ──►┤ ┤◄──
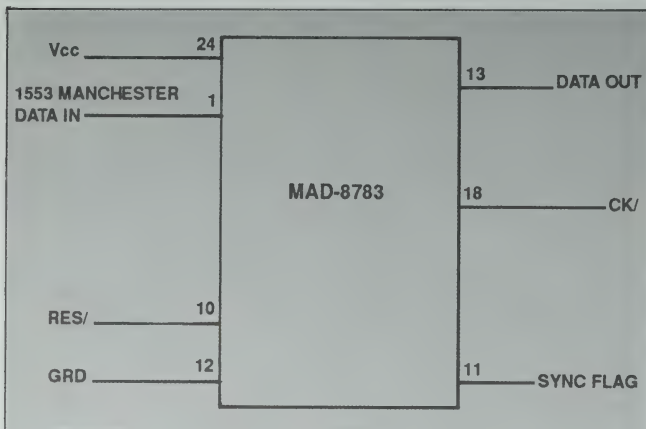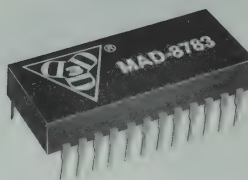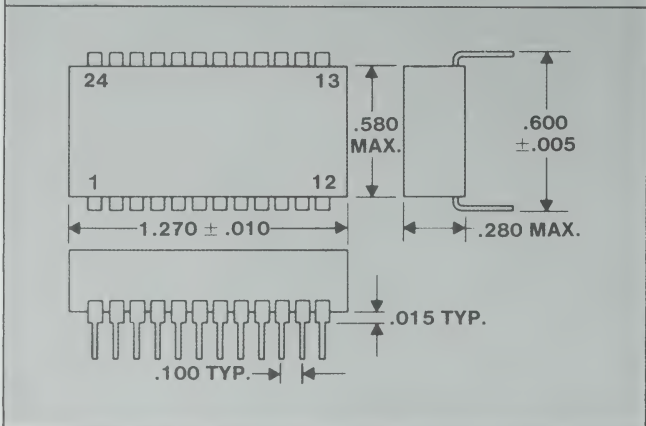
MAD-8783 Timing Waveforms

PWSYNC = 75 nsec ± 10%

PWDATA = 50 nsec ± 10%

PWDØ = 25 nsec ± 10%

PWRESET = 10 nsec min.

TSYNC = 10 nsec typ.

TDATA = 70 nsec typ.

TCK = 25 nsec typ.

**Note: The MAD will recognize as a Sync any pulse ≥ 62.5 nsec.
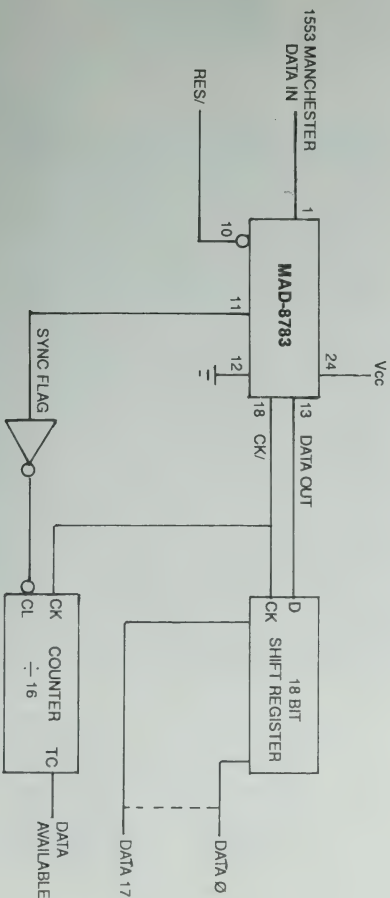
Typical Decoder Interface

Manchester Repeater

SERIES: MAR-90

(24 pins DIP)
Fast-TTL Interfaced

data delay devices, inc. ®

Description:

In today's data communication networks, it is imperative that the data be transmitted and received with a high degree of pulse and frequency fidelity. Data sent through transmission lines get degraded as it travels down the medium. For very long transmission lines, the data received may differ from the transmitted data both in frequency and duty cycle. If this shift is appreciable, data received will be incomprehensible and therefore useless.

Our MANCHESTER REPEATER MAR-90 is ideally suitable to restore the duty cycle of the original signal. It can be placed anywhere along the transmission line at regular intervals as necessary. It is very simple to implement and causes no distortion to the data format. Each unit is designed with a particular baud rate. Units with other baud rates, not listed in the P/N table, are available on request.
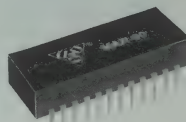
Features:

- Input/Outputs TTL buffered.
- Jitter Free Operation.
- Self-synchronizing

Applications:

- Local Area Network (LAN) Interfaces
- Ethernet BUS Interfaces
- IEEE 802 LAN Interfaces
- Fiber Optic Data Links

Specifications:

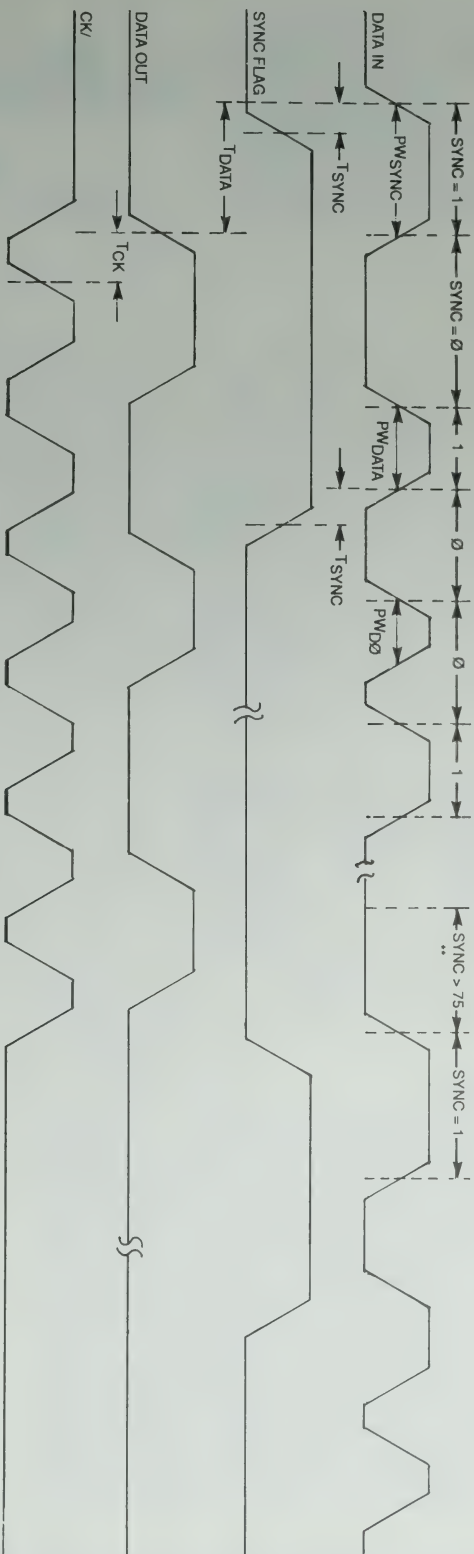- **Input signal requirement:** TTL logic
- **Output fan-out:** STD-TTL Schottky loads.
- **Operating temperature:** 0°C - 70°C. (−55°C to +125°C on request).
- **Temperature coefficient:** 100 PPM/°C.
- **Supply voltage, Vcc:** 5Vdc ±5%.
- **Power dissipation:** 350 mw typical.
- **Input frequency range:** ±5%.
- **Input pulse-width range:** ±20%.
- **Inherent delay** = 1/ (4 × baud rate).
- **Output lock-on time** = Inherent delay.
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.
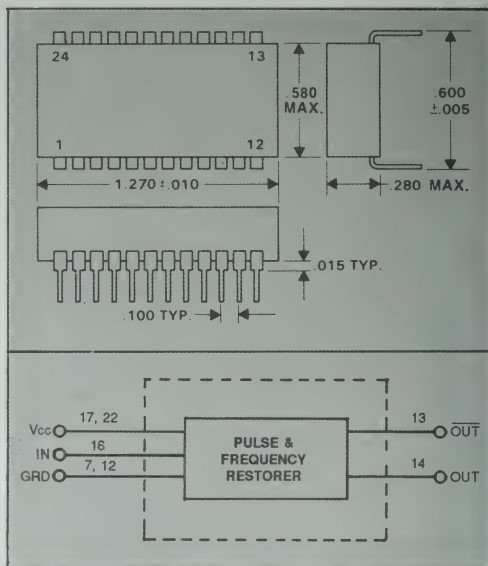
Part Number	Operating Data Rate
MAR-90-1.3	1.3 MB/S
MAR-90-4	4 MB/S
MAR-90-6	6 MB/S
MAR-90-16	16 MB/S

16 Pins-DIP-Active Filters
SERIES: 5151 & 5353

data delay devices, inc.
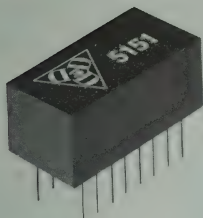
Features:

- Fits standard 16 pins DIP socket.
- No trimming required. Ready to work.
- Low profile.
- Low cost.
- Fast delivery.
- Very stable.
- Lossless.

Specifications:

- **Transfer characteristics:** Butterworth.
- **Gain in pass-band:** 0 db ± .2 db.
- **Cut-off frequency accuracy:** ±2% @ −3 db.
- **Maximum input voltage:** 10 volts peak.
- **Skirt Attenuation:** 24 db/octave.
- **DC drift:** 20uV/°C typical.
- **Supply Voltage:** ±15V typical (±9V to ±18V operational).
- **Temperature range:** 0°C to +70°C (standard); −55°C to +125°C (on request).
- **Temperature Coefficient:** .03%/°C. Better on request.
- **Power Consumption:** 200MW Maximum.

LOW-PASS FILTERS			
Part No.	3 db — Frequency (HZ)	Part No.	3 db — Frequency (HZ)
5151-1	1	5151-400	400
5151-10	10	5151-1,000	1,000
5151-20	20	5151-1,200	1,200
5151-40	40	5151-2,500	2,500
5151-50	50	5151-4,000	4,000
5151-100	100	5151-5,000	5,000
5151-200	200	5151-20,000	20,000

HIGH-PASS FILTERS			
5353-10	10	5353-2,500	2,500
5353-100	100	5353-3,250	3,250
5353-160	160	5353-4,000	4,000
5353-400	400	5353-13,000	13,000
5353-500	500	5353-16,000	16,000
5353-1,000	1,000	5353-20,000	20,000
5353-1,800	1,800		

NOTE: The above table gives only a small number of designs available. Many other designs are available on request. Any frequency from 1Hz to 25KHz can be selected. To make a part number, simply use the basic series number and cut-off frequency.
Ex.: 1. Low-pass filter, 3 db @ 9KHz
    Part No. 5151-9000
  2. High-pass filter, 3 db @ 8KHz
    Part No. 5353-8000

FUNCTION	PIN #
INPUT	1
OUTPUT	11
GND	15
V+	12
V−	8
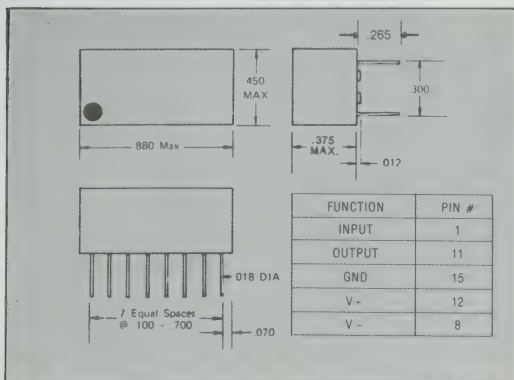
Fixed-DIP-Delay Lines
SERIES: 1502

$T_D/T_R = 3/1$

data delay devices, inc. ®

Part No.	Td (ns)	Ro (ohms)	Part No.	Td (ns)	Ro (ohms)	Part No.	Td (ns)	Ro (ohms)
1502-1	5	100	1502-19	80	200	1502-37	60	300
1502-2	10	100	1502-20	5	250	1502-38	80	300
1502-3	15	100	1502-21	10	250	1502-39	100	300
1502-4	20	100	1502-22	15	250	1502-40	10	350
1502-5	40	100	1502-23	20	250	1502-41	20	350
1502-6	5	150	1502-24	30	250	1502-42	30	350
1502-7	10	150	1502-25	40	250	1502-43	40	350
1502-8	15	150	1502-26	50	250	1502-44	50	350
1502-9	20	150	1502-27	60	250	1502-45	80	350
1502-10	30	150	1502-28	80	250	1502-46	100	350
1502-11	50	150	1502-29	100	250	1502-47	10	400
1502-12	5	200	1502-30	5	300	1502-48	20	400
1502-13	10	200	1502-31	10	300	1502-49	30	400
1502-14	15	200	1502-32	15	300	1502-50	40	400
1502-15	20	200	1502-33	20	300	1502-51	10	500
1502-16	30	200	1502-34	30	300	1502-52	20	500
1502-17	40	200	1502-35	40	300	1502-53	30	500
1502-18	60	200	1502-36	50	300			

Specifications:

- Standard 14 lead I.C. case.
- 50 vdc withstanding voltage.
- Td/tr ≥3/1.
- Impedance: 100 to 500 ohms.
- Taps available on request.
- Taps accuracy: ±5% of tap delay.
- Temperature coefficient: 100 PPM/°C.

Lead Material:
Nickel-iron alloy 42
TIN PLATE

780 MAX
.280 MAX
.290 MAX.
.015 TYP
.018 TYP
.600 ± .010
.070 MAX
.010 ± .002
.350 / .310

1 IN
5 OUT
8 GRD

Trim-DIP Delay Lines
SERIES: 1503 & 1503J

data delay devices, inc. ®

Specifications:

- Continuously variable delay.
- Multi-turn adjusting screw (40 turns approx.).
- Delay (see table).
- Impedance (see table).
- Rise-time (see table).
- Withstanding voltage: 50 Vdc.
- Temperature coefficient: 100 PPM/°C.
- Flat leads (.020 × .010).
- Resolution: .12 ns approx.
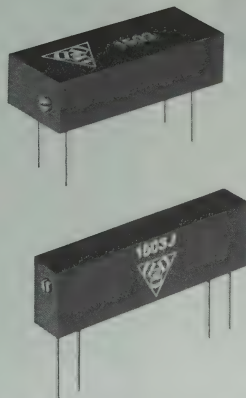
Series 1503J
Specifications: Same as 1503, except adjusting screw has 60 turns approximately.
#20 Gauge Leads

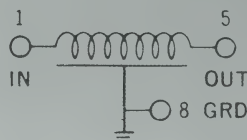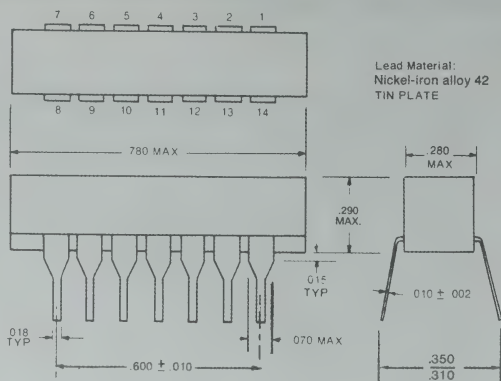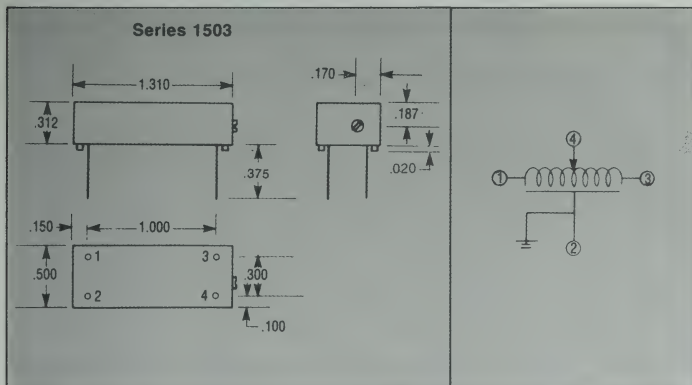| Part No.	Td (ns)	Imp. Ω	Rdc Ω	Tr (ns)
1503-15A	15	50	.7	3
1503-25A	25	50	.8	5
1503-30A	30	50	1.0	6
1503-40A	40	50	1.5	8
1503-50A	50	50	1.7	10
1503-60A	60	50	2.0	12
1503-80A	80	50	3.0	16
1503-100A	100	50	3.5	20
1503-15B	15	100	1.0	3
1503-30B	30	100	2.0	6
1503-50B	50	100	3.0	10
1503-60B	60	100	4.0	12
1503-80B	80	100	5.0	16
1503-100B	100	100	14.0	20
1503-120B	120	100	8.0	24
1503-140B	140	100	14.0	28
1503-160B	160	100	10.0	32
1503-200B	200	100	14.0	40
1503-30C	30	200	4.0	6
1503-60C	60	200	9.5	12
1503-100C	100	200	14.0	20
1503-20D	20	250	5.0	4
1503-20E	20	300	5.0	4
1503-30F	30	350	8.0	6
1503-25G	25	400	8.0	5
1503-40H	40	500	12.0	8

Series 1503

Series 1503J
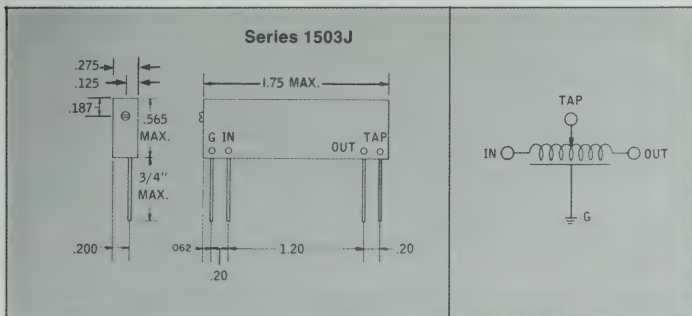
Part No.	Td (ns)	Imp. Ω	Tr (ns)	Rdc Ω
1503J-150A	150	50	22	5
1503J-250B	250	100	38	21
1503J-130C	130	200	20	21
1503J-30D	30	250	5	7
1503J-30E	30	300	5	7
1503J-40F	40	350	6	10
1503J-35G	35	400	6	10
1503J-60H	60	500	9	18

**Contact us for specific requirements.
We customize.**

Fixed-DIP Delay Lines
SERIES: 1504

$T_D/T_R = 5/1$

data delay devices, inc. ®

Features:

- **1000 Ns delay.**
- **Fast delivery.**
- **High fidelity.**
- **Low DC resistance.**
- **Standard 16 pins DIP.**
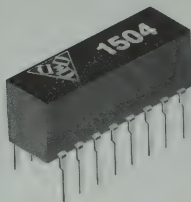
Specifications:

- **Delay:** (see table).
- **Delay accuracy:** ±5% (other tolerances on request).
- **Delay Taps:** Available on request.
- **Impedances:** (See table, others on request).
- **Impedance Accuracy:** ±10% (other tolerances on request).
- **Rise Time:** 20% of total time delay.
- **Withstanding voltage:** 50 Vdc. Min.
- **Temperature Coefficient:** 100 PPM/°C.
- **Environment:** Meets or exceeds MIL-D-23859C.

Lead Material: Nickel-iron alloy 42 TIN PLATE

.280* MAX.
.290* MAX.
.900 MAX.
.015 TYP.
.010 ±.002
.018 TYP.
.070 MAX.
.350 / .310
700 ±.010.
7 Equal spaces, each .100 ±.010.
Non-Accumulative.

1 IN — 5 OUT — 8 GRD

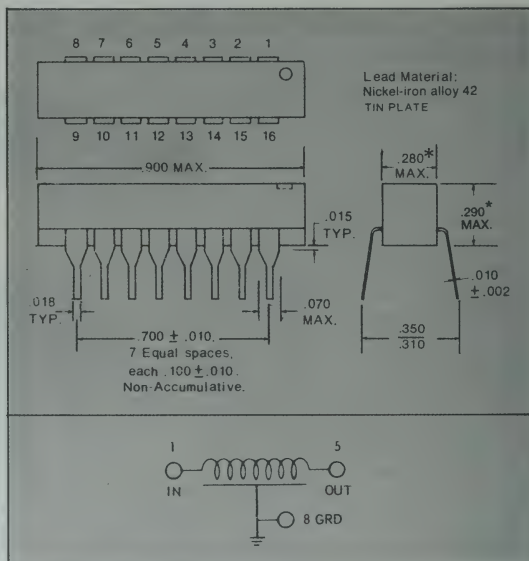| Part No.	Total Delay (ns)	Imp. Ω	Rdc Ω	Part No.	Total Delay (ns)	Imp. Ω	Rdc Ω	Part No.	Total Delay (ns)	Imp. Ω	Rdc Ω
1504-20A	20	50	1.0	1504-140C	140	200	7.0	1504-600E	600	300	40.0
1504-25A	25	50	1.0	1504-160C	160	200	7.0	1504-40F	40	400	8.5
1504-30A	30	50	1.2	1504-180C	180	200	8.5	1504-80F	80	400	9.0
1504-40A	40	50	1.5	1504-240C	240	200	9.5	1504-120F	120	400	9.0
1504-45A	45	50	1.5	1504-300C	300	200	16.0	1504-160F	160	400	16.0
1504-60A	60	50	1.5	1504-400C	400	200	18.0	1504-200F	200	400	18.0
1504-75A	75	50	1.8	1504-25D	25	250	5.0	1504-240F	240	400	20.0
1504-100A	100	50	2.0	1504-50D	50	250	5.5	1504-320F	320	400	26.0
1504-10B	10	100	1.0	1504-75D	75	250	6.0	1504-360F	360	400	28.0
1504-20B	20	100	1.5	1504-100D	100	250	7.0	1504-480F	480	400	38.0
1504-30B	30	100	1.5	1504-125D	125	250	8.0	1504-600F	600	400	45.0
1504-40B	40	100	1.8	1504-150D	150	250	8.5	1504-800F	800	400	40.0
1504-50B	50	100	2.0	1504-200D	200	250	10.0	1504-50G	50	500	6.0
1504-60B	60	100	3.0	1504-225D	225	250	11.0	1504-100G	100	500	10.0
1504-80B	80	100	3.5	1504-300D	300	250	17.0	1504-150G	150	500	16.0
1504-90B	90	100	3.5	1504-375D	375	250	20.0	1504-200G	200	500	30.0
1504-100B	100	100	4.0	1504-500D	500	250	24.0	1504-220G	220	500	31.0
1504-120B	120	100	4.0	1504-30E	30	300	5.0	1504-250G	250	500	25.0
1504-150B	150	100	5.0	1504-60E	60	300	6.0	1504-300G	300	500	26.0
1504-200B	200	100	6.0	1504-90E	90	300	7.0	1504-380G	380	500	33.0
1504-250B	250	100	7.0	1504-120E	120	300	8.0	1504-400G	400	500	42.0
1504-20C	20	200	3.0	1504-150E	150	300	9.0	1504-450G	450	500	45.0
1504-40C	40	200	4.0	1504-180E	180	300	11.0	1504-500G	500	500	55.0
1504-60C	60	200	4.5	1504-240E	240	300	16.0	*1504-600G	600	500	58.0
1504-80C	80	200	5.5	1504-270E	270	300	18.0	*1504-750G	750	500	50.0
1504-100C	100	200	6.0	1504-360E	360	300	21.0	*1504-1000G	1000	500	65.0
1504-120C	120	200	6.5	1504-450E	450	300	24.0				

* .320 MAX

Single-In-Line Delay Lines

SERIES: 1505

7 Pins SIP
5 Taps

data delay devices, inc. ®

Specifications:

- **5 Equal Taps**
- **Low Profile**
- **Meets or Exceeds:** MIL-D-23859C
- **Operating Temperature Range:** − 55°C to + 125°C
- **Storage Temperature Range:** − 55°C to + 125°C
- **Temperature Coefficient:** 100 PPM/°C
- **Dielectric Breakdown:** 50 Vdc
- **Epoxy Encapsulated**
- **Maximum Distortion @ Output:** 10%
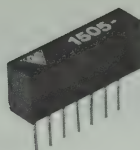
Part No.	Total Delay (ns)	Imp. (Ω)	Rdc (Ω)	Delay Per Tap (ns)	Rise Time (ns)
1505-5A	5 ± 1.0	50	.6	1 ± .3	2.0
1505-10A	10 ± 1.0	50	.6	2 ± .4	3.0
1505-20A	20 ± 1.5	50	.7	4 ± .6	6.0
1505-30A	30 ± 2.0	50	.7	6 ± 1.0	9.0
1505-40A	40 ± 2.5	50	.9	8 ± 1.5	12.0
1505-50A	50 ± 3.0	50	1.0	10 ± 1.8	15.0
1505-60A	60 ± 3.0	50	1.2	12 ± 2.0	18.0
1505-70A	60 ± 3.5	50	1.4	14 ± 2.0	21.0
1505-80A	80 ± 4.0	50	1.6	16 ± 2.0	24.0
1505-90A	90 ± 5.0	50	1.8	18 ± 3.0	27.0
1505-100A	100 ± 5.0	50	2.0	20 ± 3.0	30.0
1505-5B	5 ± 1.0	100	.7	1 ± .3	2.0
1505-10B	10 ± 1.0	100	.7	2 ± .4	3.0
1505-20B	20 ± 1.5	100	1.0	4 ± .6	6.0
1505-30B	30 ± 2.0	100	1.5	6 ± 1.0	9.0
1505-40B	40 ± 2.5	100	1.8	8 ± 1.5	12.0
1505-50B	50 ± 3.0	100	2.0	10 ± 1.8	15.0
1505-60B	60 ± 3.0	100	2.0	12 ± 2.0	18.0
1505-75B	75 ± 3.5	100	2.5	15 ± 2.0	24.0
1505-100B	100 ± 5.0	100	3.5	20 ± 3.0	30.0
1505-30C	30 ± 2.0	200	2.5	6 ± 1.0	9.0
1505-50C	50 ± 3.0	200	3.0	10 ± 1.8	15.0
1505-60C	60 ± 3.0	200	3.5	12 ± 2.0	18.0
1505-100C	100 ± 5.0	200	6.0	20 ± 3.0	30.0
1505-50G	50 ± 3.0	500	5.0	10 ± 1.8	15.0
1505-100G	100 ± 5.0	500	15.0	20 ± 3.0	30.0
1505-200G	200 ± 10.0	500	21.0	40 ± 6.0	60.0
1505-300G	300 ± 15.0	500	29.0	60 ± 8.0	90.0

Single-In-Line Delay Lines

SERIES: **1507**

14 pins SIP
10 Taps
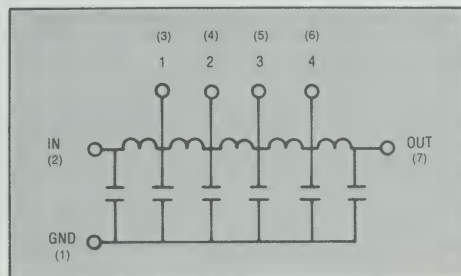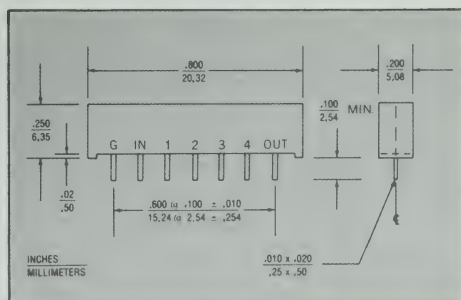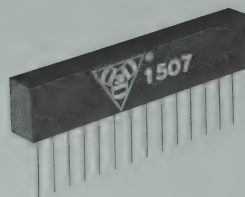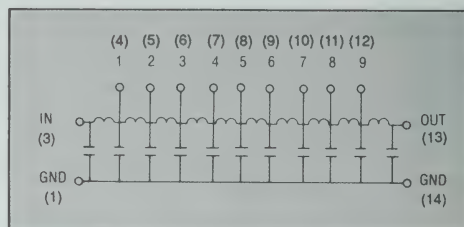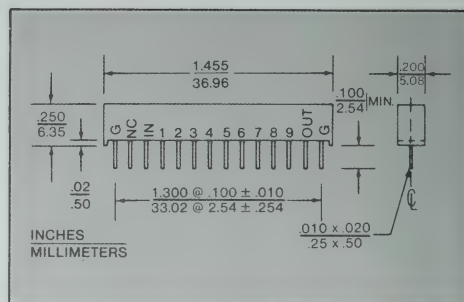
data delay devices, inc.

Specifications:

- **10 Equal Taps**
- **Low Profile**
- **Meets or Exceeds:** MIL-D-23859C
- **Operating Temperature Range:** −55°C to +125°C
- **Storage Temperature Range:** −55°C to +125°C
- **Temperature Coefficient:** 100 PPM/°C
- **Dielectric Breakdown:** 50 Vdc
- **Epoxy Encapsulated**
- **Maximum Distortion @ Output:** 10%

Part No.	Total Delay (ns)	Imp. (Ω)	Rdc (Ω)	Delay Per Tap (ns)	Rise Time (ns)
1507-20A	20 ± 2.0	50	1.0	2 ± .4	4.0
1507-40A	40 ± 2.0	50	1.5	4 ± 1.0	8.0
1507-50A	50 ± 2.5	50	1.5	5 ± 1.5	9.0
1507-100A	100 ± 5.0	50	2.0	10 ± 2.0	18.0
1507-150A	150 ± 7.5	50	3.0	15 ± 2.0	28.0
1507-200A	200 ± 10.0	50	4.0	20 ± 3.0	38.0
1507-20B	20 ± 2.0	100	1.5	2 ± .4	4.0
1507-50B	50 ± 2.5	100	2.0	5 ± 1.5	9.0
1507-100B	100 ± 5.0	100	4.0	10 ± 2.0	18.0
1507-200B	200 ± 10.0	100	6.0	20 ± 3.0	38.0
1507-250B	250 ± 13.0	100	7.0	25 ± 4.0	48.0
1507-20C	20 ± 2.0	200	3.0	2 ± .4	4.0
1507-50C	50 ± 2.5	200	4.5	5 ± 1.5	9.0
1507-100C	100 ± 5.0	200	6.0	10 ± 2.0	18.0
1507-200C	200 ± 13.0	200	9.0	20 ± 3.0	38.0
1507-50G	50 ± 2.5	500	6.0	5 ± 1.5	9.0
1507-100G	100 ± 5.0	500	10.0	10 ± 2.0	18.0
1507-200G	200 ± 10.0	500	30.0	20 ± 3.0	38.0
1507-300G	300 ± 15.0	500	30.0	30 ± 4.0	58.0
1507-500G	500 ± 25.0	500	55.0	50 ± 5.0	98.0

1.455
36.96
.200
5.08
.100
2.54 MIN
.250
6.35
G NC IN 1 2 3 4 5 6 7 8 9 OUT G
.02
.50
1.300 @ .100 ± .010
33.02 @ 2.54 ± .254
.010 x .020
.25 x .50
INCHES
MILLIMETERS

(4) (5) (6) (7) (8) (9) (10) (11) (12)
1 2 3 4 5 6 7 8 9
IN (3)
OUT (13)
GND (1)
GND (14)

Mini-Trim Delay Lines
SERIES: 1509 & 1509J

Specifications:

- Low cost unit.
- Fits standard DIP sockets.
- Continuously variable.
- 20 Turns approx.
- Resolution: .15 ns.
- Withstanding voltage: 100 Vdc.
- Temperature coefficient: 200 PPM/°C.
- Flat leads (.020 × .010).
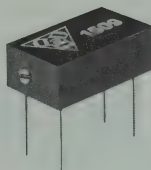
Series 1509J
Specifications: Same as 1509, except adjusting screw has 60 turns approximately.
#20 Gauge Leads
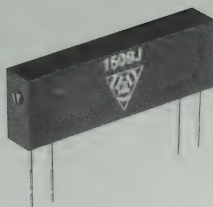
Part No.	Total Delay (ns)	Impedance (Ω)	TR (ns)	Rdc (Ω)
SERIES 1509				
1509-05B	5	100	3	.4
1509-20C	20	200	8	1.0
1509-20D	20	250	8	1.0
1509-30F	30	400	10	7.0
1509-40H	40	500	15	13.0
SERIES 1509J				
1509J-10B	10	100	4	.8
1509J-40C	40	200	9	1.5
1509J-40E	40	300	9	6.0
1509J-75F	75	400	16	12.0
1509J-80H	80	500	16	20.0

Contact us for specific requirements. We customize.

SERIES 1509
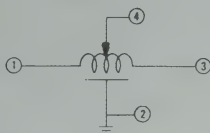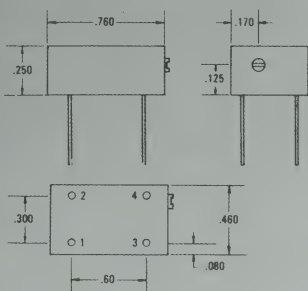
SERIES 1509J
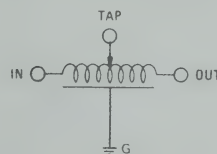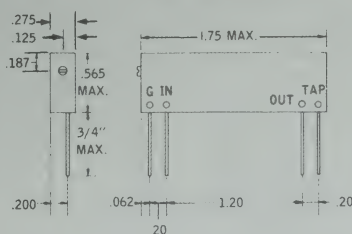
Fixed-SIP Delay Lines
1513 SERIES (HIGH FREQUENCY)

data delay devices, inc. ®

Features:
- Fast rise-time.
- 4-pins single-in-line.
- Clean signal.
- Low profile.
- Thin package.

Specifications:

- Meets or exceeds: MIL-D-23859C.
- Operating temperature: −55°C to +125°C.
- Storage temperature: −55°C to +125°C.
- Temperature coefficient: 100 PPM/°C.
- Dielectric breakdown: 50 Vdc.
- Epoxy encapsulated.
- Distortion @ output: 10% max.
- Rise-time: 1 ns or 20% of T$_D$
  (whichever is greater)
- Delay tolerance: 5% or 1 ns
  whichever is greater
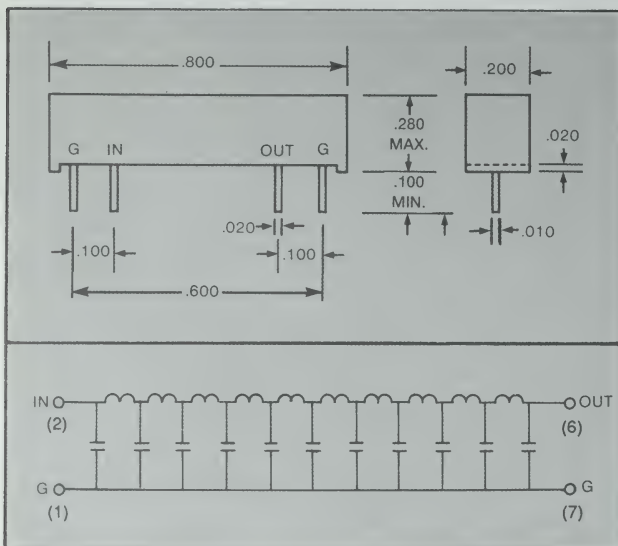
Part No.	Delay (ns)	Impedance Ω
1513-2.5A	2.5	50
1513-5A	5	50
1513-10A	10	50
1513-15A	15	50
1513-20A	20	50
1513-25A	25	50
1513-30A	30	50
1513-40A	40	50
1513-50A	50	50
1513-60A	60	50
1513-70A	70	50
1513-80A	80	50
1513-90A	90	50
1513-100A	100	50
1513-3.5Y	3.5	75
1513-7.5Y	7.5	75
1513-15Y	15	75
1513-22.5Y	22.5	75
1513-30Y	30	75
1513-37.5Y	37.5	75
1513-45Y	45	75
1513-60Y	60	75
1513-75Y	75	75
1513-90Y	90	75
1513-105Y	105	75
1513-120Y	120	75
1513-135Y	135	75
1513-150Y	150	75
1513-5B	5	100
1513-10B	10	100
1513-20B	20	100
1513-30B	30	100
1513-40B	40	100
1513-50B	50	100
1513-60B	60	100
1513-80B	80	100
1513-100B	100	100
1513-120B	120	100
1513-140B	140	100
1513-150B	150	100

Features:
- **Fast rise-time.**
- **4-pins single-in-line.**
- **Clean signal.**
- **Low profile.**
- **Thin package.**

Specifications:
- **Meets or exceeds:** MIL-D-23859C.
- **Operating temperature:** −55°C to +125°C.
- **Storage temperature:** −55°C to +125°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Dielectric breakdown:** 50 Vdc.
- **Epoxy encapsulated.**
- **Distortion @ output:** 10% max.
- **Rise-time:** 1 ns or 20% of T_D (whichever is greater)
- **Delay tolerance:** 5% or 1 ns (whichever is greater)

Part No.	Delay (ns)	Impedance Ω
1514-2.5A	2.5	50
1514-5A	5	50
1514-10A	10	50
1514-15A	15	50
1514-20A	20	50
1514-25A	25	50
1514-30A	30	50
1514-40A	40	50
1514-50A	50	50
1514-60A	60	50
1514-70A	70	50
1514-80A	80	50
1514-90A	90	50
1514-100A	100	50
1514-3.5Y	3.5	75
1514-7.5Y	7.5	75
1514-15Y	15	75
1514-22.5Y	22.5	75
1514-30Y	30	75
1514-37.5Y	37.5	75
1514-45Y	45	75
1514-60Y	60	75
1514-75Y	75	75
1514-90Y	90	75
1514-105Y	105	75
1514-120Y	120	75
1514-135Y	135	75
1514-150Y	150	75
1514-5B	5	100
1514-10B	10	100
1514-20B	20	100
1514-30B	30	100
1514-40B	40	100
1514-50B	50	100
1514-60B	60	100
1514-80B	80	100
1514-100B	100	100
1514-120B	120	100
1514-140B	140	100
1514-150B	150	100
1514-50D	50	250
1514-70D	70	250
1514-120D	120	250
1514-130D	130	250
1514-150D	150	250
1514-170D	170	250
1514-270D	270	250
1514-70E	70	300
1514-140E	140	300
1514-45G	45	500
1514-50G	50	500
1514-80G	80	500
1514-100G	100	500
1514-190G	190	500
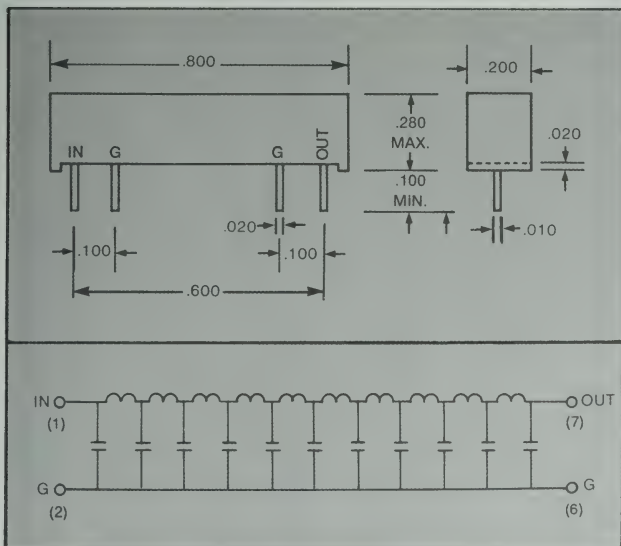
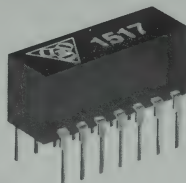# 5 TAPS-DIP Delay Lines
SERIES: 1517

$T_D/T_R = 3/1$

data delay devices, inc. ®

Features:

- 5 Taps.
- Standard 14 pins DIP case.
- Low cost.
- Fast Delivery.

Specifications:

- **Delay accuracy:** ±5% (others on request).
- **No. taps:** 5 Equally spaced taps.
- **Taps accuracy:** ±5% of tap delay.
- **Impedance tolerance:** ±10% (others on request).
- **Rise-Time:** 30% of time delay.
- **Withstanding voltage:** 50 Vdc. Min.
- **Temperature coefficient:** 100 PPM/°C.
- **Environment:** Meets or exceeds MIL-D-23859C.
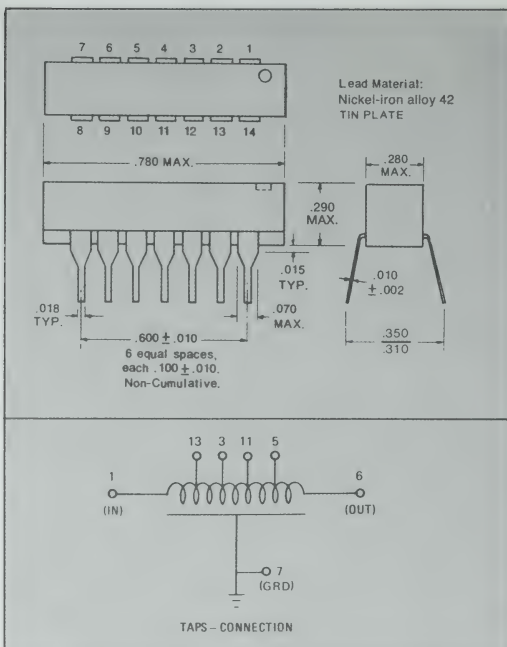
Part No.	Total Delay (ns)	Imp. (Ω)	Rdc (Ω)
1517-10A	10	50	0.6
1517-15A	15	50	0.6
1517-20A	20	50	0.7
1517-30A	30	50	0.7
1517-40A	40	50	0.9
1517-5B	5	100	0.5
1517-10B	10	100	0.7
1517-15B	15	100	0.7
1517-20B	20	100	0.9
1517-25B	25	100	1.0
1517-30B	30	100	1.5
1517-40B	40	100	1.8
1517-50B	50	100	2.0
1517-60B	60	100	2.0
1517-75B	75	100	2.5
1517-10C	10	200	1.5
1517-20C	20	200	2.0
1517-30C	30	200	2.5
1517-40C	40	200	3.0
1517-50C	50	200	3.0
1517-60C	60	200	3.5
1517-80C	80	200	3.5
1517-90C	90	200	5.0
1517-120C	120	200	5.0
1517-150C	150	200	8.0
1517-25D	25	250	2.5
1517-37D	37	250	3.0
1517-50D	50	250	3.5
1517-60D	60	250	4.0
1517-75D	75	250	4.0
1517-100D	100	250	5.0
1517-150D	150	250	8.5
1517-15E	15	300	2.5
1517-30E	30	300	3.0
1517-50E	50	300	4.0
1517-60E	60	300	4.0
1517-75E	75	300	4.5
1517-90E	90	300	5.5
1517-120E	120	300	8.0
1517-130E	130	300	9.0
1517-180E	180	300	11.0
1517-220E	220	300	13.0
1517-20F	20	400	4.5
1517-40F	40	400	5.0
1517-60F	60	400	5.0
1517-80F	80	400	8.0
1517-100F	100	400	9.0
1517-120F	120	400	10.0
1517-160F	160	400	13.0
1517-180F	180	400	14.0
1517-240F	240	400	19.0
1517-300F	300	400	23.0
1517-25G	25	500	3.0
1517-50G	50	500	5.0
1517-75G	75	500	8.0
1517-100G	100	500	15.0
1517-125G	125	500	9.0
1517-150G	150	500	13.0
1517-200G	200	500	21.0
1517-225G	225	500	23.0
1517-300G	300	500	29.0

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.780 MAX.
.280 MAX.
.290 MAX.
.015 TYP.
.010 ± .002
.018 TYP.
.070 MAX.
.350
.310
.600 ± .010
6 equal spaces,
each .100 ± .010.
Non-Cumulative.

13 3 11 5

1 (IN)   6 (OUT)

7 (GRD)

TAPS – CONNECTION

10 Taps-DIP Delay Lines
SERIES: 1519

$T_D/T_R = 5/1$

data delay devices, inc. ®

Specifications:

- **Delay accuracy:** ±5% (others on request).
- **No. taps:** 10 Equally spaced taps.
- **Taps accuracy:** ±5% of tap delay.
- **Impedance tolerance:** ±10% (others on request).
- **Rise-Time:** 20% of time delay.
- **Withstanding voltage:** 50 Vdc. Min.
- **Temperature coefficient:** 100 PPM/°C.
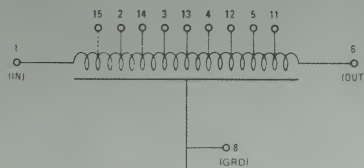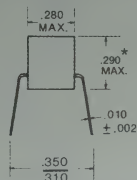- **Environment:** Meets or exceeds MIL-D-23859C.

Features:

- **1000 Ns delay.**
- **10 Taps.**
- **Standard 16 pins DIP cases.**
- **Low D.C. resistance.**
- **Fast delivery.**

Lead Material:
Nickel-iron alloy 42
TIN PLATE

.900 MAX.
.015 TYP.
.018 TYP.
.070 MAX.
.700 ± .010.
7 Equal spaces,
each .100 ± .010.
Non-Accumulative.

.280 MAX.
.290 MAX.
.010 ± .002
.350 / .310
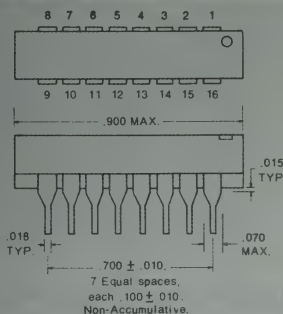
Part No.	Total Delay (ns)	Imp. (Ω)	Rdc (Ω)	Part No.	Total Delay (ns)	Imp. (Ω)	Rdc (Ω)	Part No.	Total Delay (ns)	Imp. (Ω)	Rdc (Ω)
1519-20A	20	50	1.0	1519-100C	100	200	6.0	1519-360E	360	300	21.0
1519-25A	25	50	1.0	1519-120C	120	200	6.5	1519-450E	450	300	25.0
1519-30A	30	50	1.2	1519-160C	160	200	7.0	1519-600E	600	300	40.0
1519-40A	40	50	1.5	1519-180C	180	200	8.5	1519-40F	40	400	8.5
1519-45A	45	50	1.5	1519-200C	200	200	9.0	1519-80F	80	400	9.0
1519-50A	50	50	1.5	1519-240C	240	200	9.5	1519-120F	120	400	9.0
1519-60A	60	50	1.5	1519-300C	300	200	16.0	1519-160F	160	400	16.0
1519-75A	75	50	1.8	1519-400C	400	200	16.0	1519-200F	200	400	18.0
1519-100A	100	50	2.0	1519-50D	50	250	5.5	1519-240F	240	400	20.0
1519-10B	10	100	1.0	1519-75D	75	250	6.0	1519-320F	320	400	26.0
1519-20B	20	100	1.5	1519-100D	100	250	7.0	1519-360F	360	400	28.0
1519-30B	30	100	1.5	1519-125D	125	250	8.0	1519-480F	480	400	38.0
1519-40B	40	100	1.8	1519-150D	150	250	8.5	1519-600F	600	400	45.0
1519-50B	50	100	2.0	1519-200D	200	250	10.0	*1519-800F	800	400	40.0
1519-60B	60	100	3.0	1519-225D	225	250	11.0	1519-50G	50	500	6.0
1519-80B	80	100	3.5	1519-300D	300	250	17.0	1519-100G	100	500	10.0
1519-90B	90	100	3.5	1519-375D	375	250	20.0	1519-150G	150	500	16.0
1519-100B	100	100	4.0	1519-500D	500	250	24.0	1519-200G	200	500	30.0
1519-120B	120	100	4.0	1519-30E	30	300	5.0	1519-250G	250	500	18.0
1519-150B	150	100	5.0	1519-60E	60	300	6.0	1519-300G	300	500	26.0
1519-200B	200	100	6.0	1519-90E	90	300	7.0	1519-400G	400	500	42.0
1519-250B	250	100	7.0	1519-120E	120	300	8.0	1519-450G	450	500	45.0
1519-20C	20	200	3.0	1519-150E	150	300	9.0	1519-500G	500	500	55.0
1519-40C	40	200	4.0	1519-180E	180	300	11.0	*1519-600G	600	500	58.0
1519-60C	60	200	4.5	1519-240E	240	300	16.0	*1519-750G	750	500	50.0
1519-80C	80	200	5.5	1519-270E	270	300	18.0	*1519-1000G	1000	500	65.0

*.320 MAX.

PICO Seconds Delay Lines
SERIES: 2020
6 pins SIP

data delay devices, inc. ®

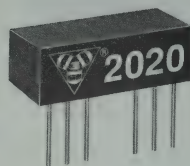| Part No.	Delay (ps)	Impedance (Ω)
2020-100	100	50
2020-150	150	50
2020-200	200	50
2020-250	250	50
2020-300	300	50
2020-350	350	50
2020-400	400	50
2020-500	500	50
2020-600	600	50
2020-700	700	50
2020-800	800	50
2020-900	900	50
2020-1000	1000	50
2020-1100	1100	50
2020-1200	1200	50
2020-1300	1300	50
2020-1400	1400	50
2020-1500	1500	50
2020-1700	1700	50
2020-1750	1750	50

Description:

The ever increasing speed of today's computers and system designs demands that propagation delays due to integrated circuit, printed circuit board lay-out and stray capacitance be compensated without reducing the system speed.
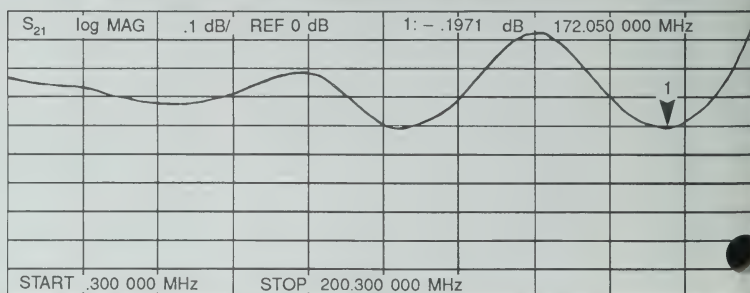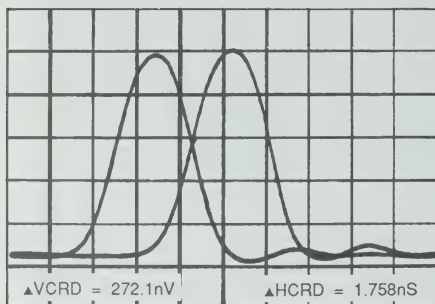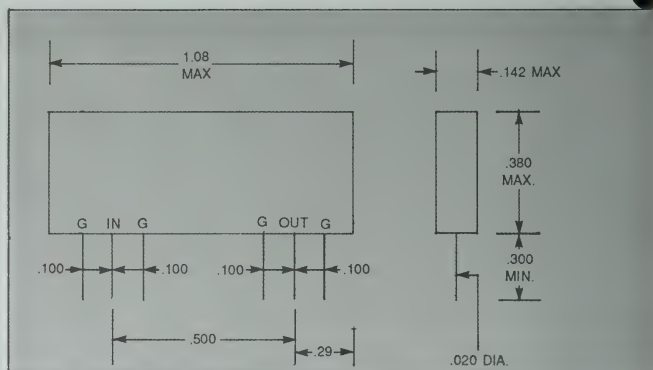
Delay line Series 2020 was developed specifically to address these requirements. The uniform construction guarantees high fidelity of signal reproduction, band-widths in excess of 350 MHZ, and consistent delay tolerance from every production lot. In many cases these units can be direct replacements of coaxial cable, thus affording reduction of cost, weight and volume. Other applications include super computers and automated test equipment.

Specifications:

- **Delay:** Fixed.
- **Delay tolerance:** 2% or 10 ps.
- **Frequency response:** Greater than 350 MHZ.
- **Ripple in pass-band:** Approximately .2 db.
- **Temperature range:** −65 to +125°C.
- **Temperature coefficient:** <100 PPM/°C.
- **Dielectric breakdown:** >500 V.
- **Meets or exceeds MIL-D-23859C.**
- **Epoxy encapsulated.**

▲VCRD = 272.1nV   ▲HCRD = 1.758nS

S_{21} log MAG   .1 dB/   REF 0 dB   1: − .1971 dB   172.050 000 MHz

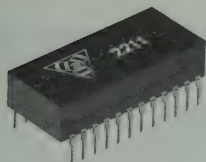START .300 000 MHz   STOP 200.300 000 MHz
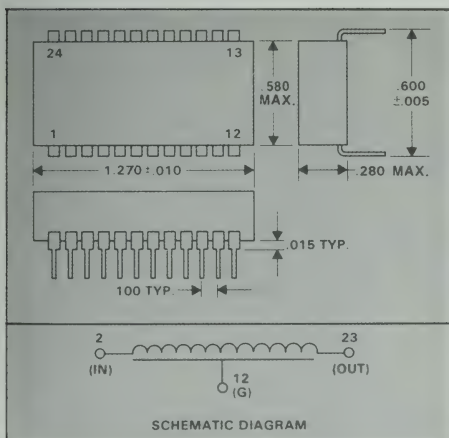
Fixed-DIP Delay Lines

SERIES: 2211

$T_D/T_R = 10/1$

data delay devices, inc. ®

Specifications:

- Standard 24 pins DIP.
- TTL and DTL compatible.
- Td/Tr = 10/1
- Delay tolerance: +5% or 1 ns whichever is greater.
- Temperature coefficient: 100 PPM/° C.
- Temperature range: −55°C to +125°C.
- Dielectric breakdown: 50 Vdc.
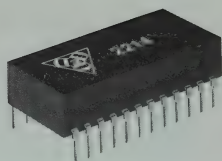- Meets or exceeds MIL-D-23859C.
- Epoxy encapsulated.

Part No.	Impedance (Ω)	Total Delay (ns)	Rdc (Ω)
2211-50A	50	50	3.2
2211-60A	50	60	3.5
2211-80A	50	80	5.0
2211-100A	50	100	6.0
2211-150A	50	150	6.0
2211-50B	100	50	6.0
2211-60B	100	60	6.0
2211-80B	100	80	6.5
2211-100B	100	100	7.0
2211-150B	100	150	8.0
2211-200B	100	200	8.5
2211-300B	100	300	11.0
2211-400B	100	400	12.0
2211-40C	200	40	7.0
2211-80C	200	80	8.0
2211-120C	200	120	10.0
2211-200C	200	200	13.0
2211-300C	200	300	12.0
2211-400C	200	400	15.0
2211-500C	200	500	17.0
2211-600C	200	600	23.0
2211-50D	250	50	7.0
2211-100D	250	100	10.0
2211-150D	250	150	12.0
2211-180D	250	180	14.0
2211-200D	250	200	22.0
2211-250D	250	250	21.0
2211-300D	250	300	23.0
2211-380D	250	380	25.0
2211-400D	250	400	26.0
2211-500D	250	500	30.0
2211-600D	250	600	37.0
2211-750D	250	750	40.0
2211-200G	500	200	20.0
2211-300G	500	300	37.0
2211-400G	500	400	40.0
2211-500G	500	500	45.0
2211-600G	500	600	52.0
2211-800G	500	800	80.0
2211-1000G	500	1000	100.0
2211-1200G	500	1200	110.0
2211-1500G	500	1500	130.0
2211-2000G	500	2000	156.0

.580 MAX.

.600 ±.005

1.270 ±.010

.280 MAX.

.015 TYP.

100 TYP.

2 (IN)   23 (OUT)

12 (G)

SCHEMATIC DIAGRAM

20 Taps-DIP Delay Lines

SERIES: 2214

$T_D/T_R = 10/1$

Part No.	Impedance (Ω)	Total Delay (ns)	Tap Increment (ns)	Rdc (Ω)
2214-50A	50	50	2.5	3.2
2214-60A	50	60	3.0	3.6
2214-80A	50	80	4.0	5.0
2214-100A	50	100	5.0	6.0
2214-150A	50	150	7.5	6.0
2214-200A	50	200	10.0	7.0
2214-50B	100	50	2.5	6.0
2214-60B	100	60	3.0	6.0
2214-80B	100	80	4.0	6.5
2214-100B	100	100	5.0	7.0
2214-150B	100	150	7.5	8.0
2214-200B	100	200	10.0	8.5
2214-300B	100	300	15.0	11.0
2214-400B	100	400	20.0	12.0
2214-40C	200	40	2.0	7.0
2214-80C	200	80	4.0	8.0
2214-120C	200	120	6.0	10.0
2214-200C	200	200	10.0	13.0
2214-300C	200	300	15.0	12.0
2214-400C	200	400	20.0	15.0
2214-500C	200	500	25.0	17.0
2214-600C	200	600	30.0	23.0
2214-800C	200	800	40.0	38.0
2214-50D	250	50	2.5	7.0
2214-100D	250	100	5.0	10.0
2214-150D	250	150	7.5	12.0
2214-200D	250	200	10.0	22.0
2214-250D	250	250	12.5	21.0
2214-300D	250	300	15.0	23.0
2214-400D	250	400	20.0	26.0
2214-500D	250	500	25.0	30.0
2214-600D	250	600	30.0	37.0
2214-800D	250	800	40.0	41.0
2214-1000D	250	1000	50.0	47.0
2214-200G	500	200	10.0	20.0
2214-300G	500	300	15.0	37.0
2214-400G	500	400	20.0	40.0
2214-500G	500	500	25.0	45.0
2214-600G	500	600	30.0	52.0
2214-800G	500	800	40.0	80.0
2214-1000G	500	1000	50.0	100.0
2214-1200G	500	1200	60.0	110.0
2214-1500G	500	1500	75.0	130.0
2214-2000G	500	2000	100.0	156.0

Specifications:

- **20 Equally spaced taps.**
- **TTL and DTL compatible.**
- **Td/Tr = 10/1**
- **Delay tolerance: +5% or 1 ns whichever is greater.**
- **Tap tolerance: ±5% or 1 ns whichever is greater.**
- **Temperature coefficient: 100 PPM/° C.**
- **Temperature range: −55°C to +125°C.**
- **Dielectric breakdown: 50 Vdc.**
- **Meets or exceeds MIL-D-23859C.**
- **Epoxy encapsulated.**

SCHEMATIC DIAGRAM

PACKAGES OUTLINE DIMENSIONS

A1

A2

A3

A4

C1

C2
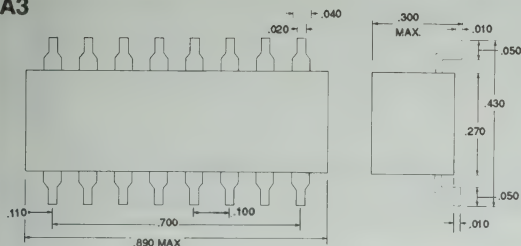
PACKAGES OUTLINE DIMENSIONS

C3

E1

† or case stand-offs

C5

E2

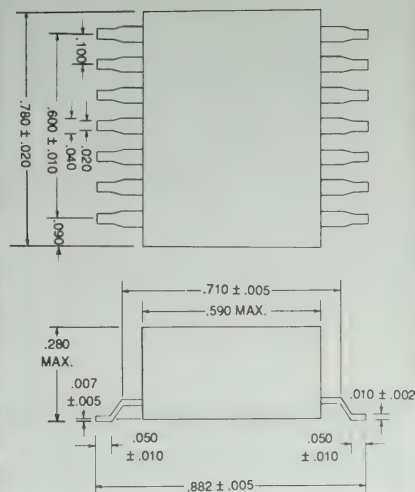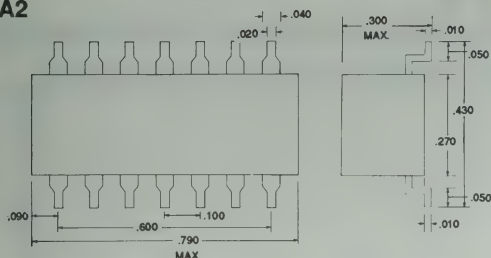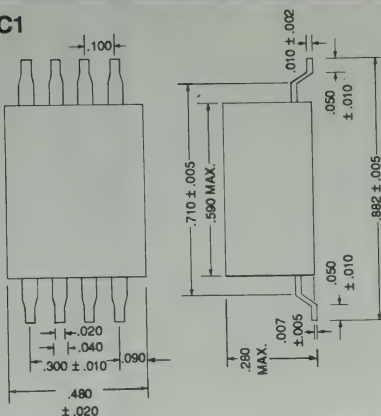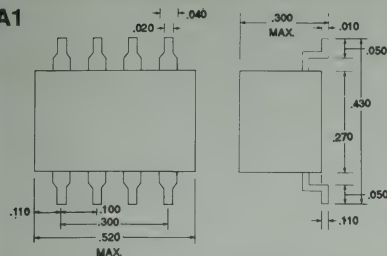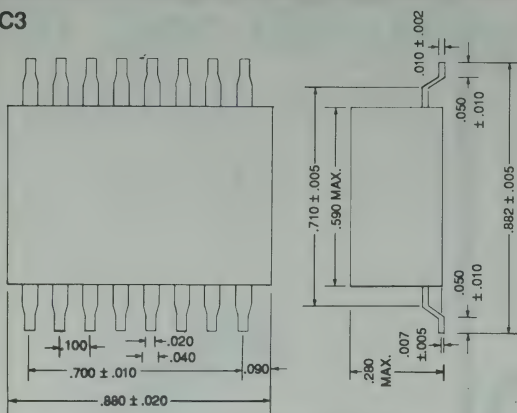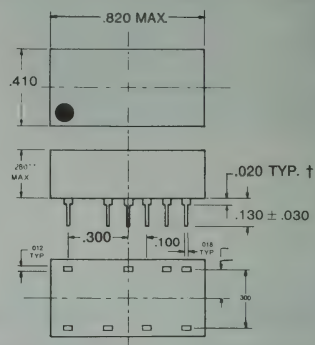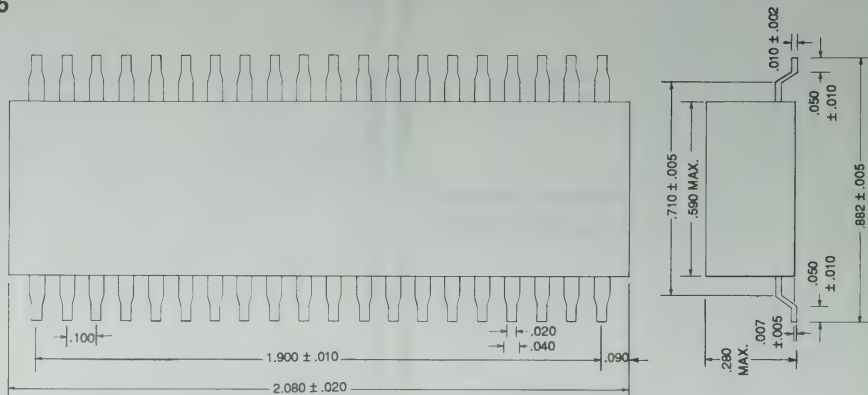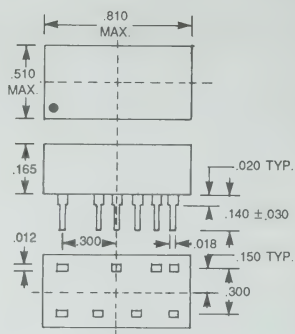## D2
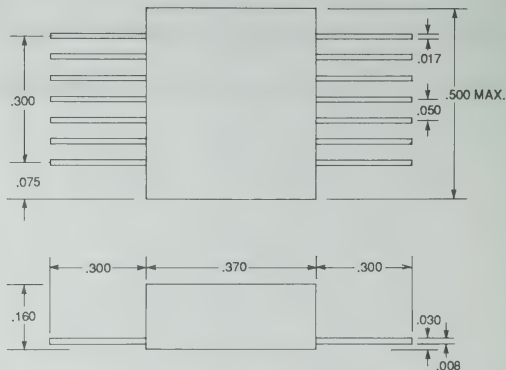
PACKAGES OUTLINE DIMENSIONS

C4
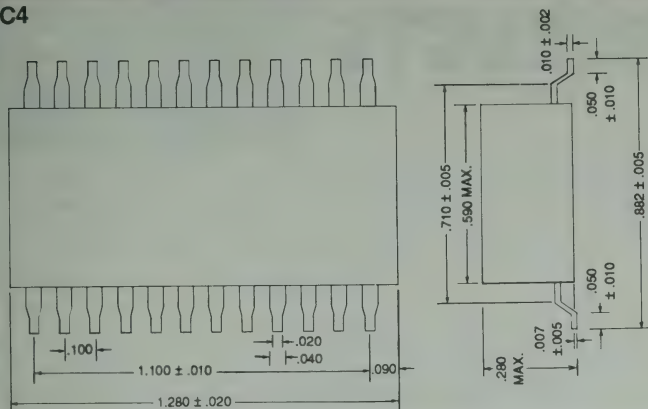
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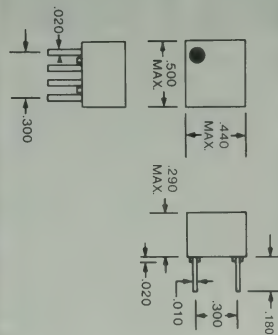
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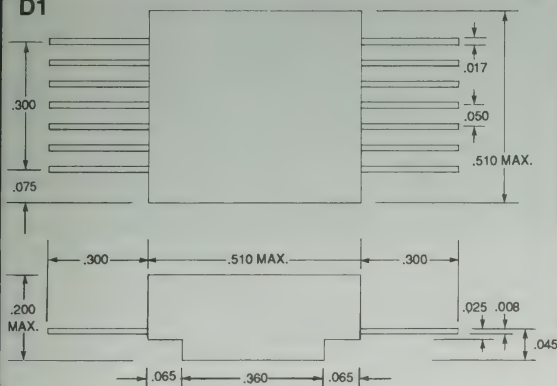
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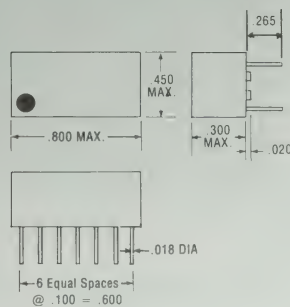
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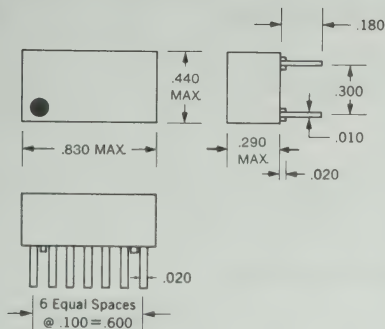
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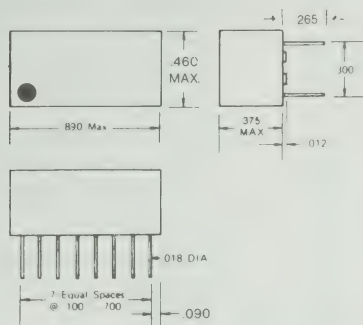
MILITARY PRODUCTS

data delay devices, inc. ®

Most of Data Delay Devices delay line products are available in military version. They are identified by adding an "M" after the Part Number.

Example:

DDU-4-5100   Commercial
DDU-4-5100M   Military

The Military Delay Line Products Feature The Following:

1. All components meet their respective MIL-Specs.
2. The internal IC's are packaged in ceramic case and are screened to MIL-STD-883.
3. Operate over full military temperature range of –55°C to +125°C.
4. Meet or exceed all the environmental requirements of MIL-D-23859.
5. 100% screening is performed for:
   a. Thermal Shock – 15 cycles, –55°C to +125°C.
   b. Burn-In – 196 hours @ +125°C with power applied.
6. Complete qualification tests and test report available at cost.

APPLICATION NOTES no. 02

HIGH PRECISION – HIGH FREQUENCY PROGRAMMABLE DELAY LINES

by Nino Lupi, President

Digital delay lines are very precise time devices and operate over a wide band of high frequency rates and pulse-widths.

This high accuracy is maintained provided the pulse-width is greater than the total delay of the delay line and the rep rate is greater than 2X pulse-width. When the pulse-width and rep rate decrease below the total delay of the delay line then small errors in delay tolerance occur due to the switching of the incoming signal lining up with the tap delay used. (Refer to DDD application no. 01 for explanation.)

Data Delay Devices has developed a scheme to circumvent this situation and thus be able to operate delay lines with pulse-widths and rep rates much lower than total time delay of the delay line without losing the time accuracy. It is a very powerful design for digitally programmable delay lines because there are many steps of delay change. Each delay step has to be compensated. This approach is valid in applications where the frequency and pulse-width are kept constant. However, compensation at multiple frequencies can be accommodated.

Data Delay Devices is presently building programmable delay lines of the series PDU-8600 with actual results given below:

Programmable Delay Line Specs:

Model PDU-8600
No. bits: 6
Step increment: .5 ns
Linearity: ± .3 ns
Step increment accuracy: ± .3 ns
Operating temperature: -55˚C to +125˚C

Delay variation: Monotonic
Reversals: None
Operating frequency: 60 Mhz
Logic family: 10KH ECL
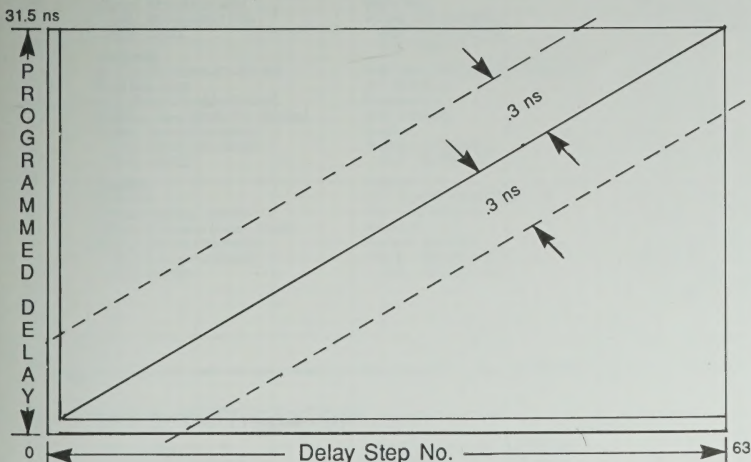
Positive deviation = .2 ns
Negative deviation = −.29 ns
Total deviation = 0 ns
Number of reversal = 0
Number of out of tolerance steps = 0

Step No.	T_D (Actual) (ns)	Deviation (ns)
0	0	0
1	.48	.02
2	1.1	−.1
3	1.5	0
4	2.04	−.04
5	2.54	−.04
6	3.01	−.01
7	3.59	−.09
8	3.96	.04
9	4.42	.08
10	5.1	−.1
11	5.52	−.02
12	6.03	−.02
13	6.57	−.07
14	6.93	.07
15	7.65	−.15
16	8.2	−.2
17	8.58	−.08
18	8.97	.03
19	9.37	.13
20	9.8	.2
21	10.32	.18
22	11.1	−.1
23	11.3	.2
24	12.01	−.01
25	12.43	.07
26	13.11	−.11
27	13.54	−.04
28	13.99	.02
29	14.48	.02
30	14.82	.18
31	15.45	.05
32	16.29	−.29
33	16.76	−.26
34	17.16	−.16
35	17.64	−.14
36	18.17	−.17
37	18.77	−.27
38	19.04	−.04
39	19.56	−.06
40	20.01	−.01
41	20.48	.02
42	21.18	−.18
43	21.6	−.1
44	22.12	−.12
45	22.65	−.15
46	23.02	−.02
47	23.56	−.06
48	24.2	−.2
49	24.68	−.18
50	25.09	−.09
51	25.51	−.01
52	26.02	−.02
53	26.6	−.1
54	26.84	.16
55	27.34	.16
56	28.04	−.04
57	28.46	.04
58	28.85	.15
59	29.67	−.17
60	30.14	−.14
61	30.64	−.14
62	30.83	.17
63	31.37	.13

31.5 ns

PROGRAMMED DELAY

.3 ns

.3 ns

0 ← Delay Step No. → 63

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U.S.A. REPRESENTATIVES

NORTHERN CALIFORNIA
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JAY MARKETING ASSOC.
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FAX: 714-581-1211

San Fernando Office
Phone: 805-522-8161
FAX: 805-527-7181

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FAX: 713-820-3219

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Dallas, TX 75244
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FAX: 214-702-8568

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Phone: 205-533-9108
FAX: 205-533-4667
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Medford, NJ 08055
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FAX: 609-953-1238

Pennsylvania Office
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P.O. Box 326
Exton, PA 19341
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Suite 3D
St. Charles, IL 60174
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FAX: 708-584-6990

CANADA

SOURCE ELECTRONICS
7050A Bramalea Road Unit 21
Mississauga, Ontario L5S 1T1
Phone: 416-676-0830
FAX: 416-676-0844

OTTAWA OFFICE
118 Borga Crescent
Ottawa, Ontario K1T 2E2
Phone: 613-737-7580
FAX: 613-731-2376

FOREIGN REPRESENTATIVES

WEST GERMANY
TELEMETER ELECTRONIC, GMBH
Posthof #4
8850 Donauworth, West Germany
Phone: 011-49-906-4091
FAX: 011-49-906-21706
TLX: 51856

ENGLAND
B.F.I. ELECTRONICS LIMITED
Burnt Ash Road
Quarrywood Industrial Estates
Aylesford, Kent ME20-7NA, England
Phone: 011-44-622-882467
FAX: 011-44-622-882469
TLX: 965757

FRANCE
PYRECAP
5, Place Salvador Allende
F-91124 Palaiseau Cedex, France
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FAX: 011-33-1-69205275
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ITALY
EXHIBO S.P.A.
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20052 Monza
Milan, Italy
Phone: 011-39-738021
FAX: 011-39-360280
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JET BENELUX
Opperjacht 9
3078 Everberg
Belgium
Phone: 02-7592101
FAX: 02-7593418

KOREA
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7000 S.W. Hampton St.
Suite 128
Portland, OR 97223
Phone: 503-624-0315
FAX: 503-624-0735

SWEDEN
AB GOSTA BACKSTROM
Alstromergatan 22
Box 12009
102 21 Stockholm, Sweden
Phone: 011-8-54-1080
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Herzlia, 46103
Israel
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Telex: 43269

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Tokyo, Japan
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FAX: 011-81-32353663
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Equivalents Millimeters to Inches

MM	INCH	MM	INCH	MM	INCH	MM	INCH	MM	INCH	MM	INCH	MM	INCH	MM	INCH
0.001	.000039	0.9	.0354	2.3	.0906	4.6	.1811	7.9	.3110	15	.5906	39	1.5364	70	2.7560
0.002	.000079	0.95	.0374	2.35	.0925	4.7	.1850	8	.3150	15.5	.6102	40	1.5748	71	2.7953
0.0025	.0001	1	.0394	2.36	.0929	4.75	.1870	8.1	.3189	16	.6299	41	1.6142	72	2.8346
0.003	.000118	1.05	.0413	2.4	.0945	4.8	.1890	8.2	.3228	16.5	.6496	42	1.6535	73	2.8740
0.004	.000157	1.06	.0417	2.45	.0965	4.9	.1929	8.3	.3268	17	.6693	43	1.6929	74	2.9134
0.005	.000197	1.1	.0433	2.5	.0984	5	.1968	8.4	.3307	17.5	.6890	44	1.7323	75	2.9528
0.006	.000236	1.12	.0441	2.55	.1004	5.1	.2008	8.5	.3346	18	.7087	45	1.7717	76	2.9921
0.007	.000276	1.15	.0453	2.6	.1024	5.2	.2047	8.6	.3386	18.5	.7283	46	1.8110	77	3.0315
0.008	.000315	1.18	.0465	2.65	.1043	5.3	.2087	8.7	.3425	19	.7480	47	1.8504	78	3.0709
0.009	.000354	1.2	.0472	2.7	.1063	5.4	.2126	8.8	.3465	19.5	.7677	48	1.8898	79	3.1102
0.01	.000394	1.25	.0492	2.75	.1083	5.5	.2165	8.9	.3504	20	.7874	49	1.9291	80	3.1496
0.02	.00079	1.3	.0512	2.8	.1102	5.6	.2205	9	.3543	20.5	.8071	50	1.9685	81	3.1890
0.025	.001	1.32	.0520	2.9	.1142	5.7	.2244	9.1	.3583	21	.8268	51	2.0079	82	3.2283
0.03	.00118	1.35	.0531	3	.1181	5.8	.2283	9.2	.3622	21.5	.8465	52	2.0472	83	3.2677
0.04	.00157	1.4	.0551	3.1	.1220	5.9	.2323	9.3	.3661	22	.8661	53	2.0866	84	3.3071
0.05	.00197	1.45	.0571	3.15	.1240	6	.2362	9.4	.3701	22.5	.8858	54	2.1260	85	3.3465
0.06	.00236	1.5	.0591	3.2	.1260	6.1	.2401	9.5	.3740	23	.9055	55	2.1654	86	3.3858
0.07	.00276	1.55	.0610	3.3	.1299	6.2	.2441	9.6	.3780	23.5	.9252	56	2.2047	87	3.4252
0.08	.00315	1.6	.0630	3.35	.1319	6.3	.2480	9.7	.3819	24	.9449	57	2.2441	88	3.4646
0.09	.00354	1.65	.0650	3.4	.1339	6.4	.2520	9.8	.3858	24.5	.9646	58	2.2835	89	3.5039
0.1	.00394	1.7	.0669	3.5	.1378	6.5	.2559	9.9	.3898	25	.9843	59	2.3228	90	3.5433
0.2	.0079	1.75	.0689	3.55	.1400	6.6	.2598	10	.3837	26	1.0236	60	2.3622	91	3.5827
0.3	.0118	1.8	.0709	3.6	.1417	6.7	.2638	10.2	.4016	27	1.0630	61	2.4016	92	3.6220
0.35	.0138	1.85	.0728	3.7	.1457	6.8	.2677	10.3	.4055	28	1.1024	62	2.4409	93	3.6614
0.4	.0157	1.9	.0748	3.75	.1477	6.9	.2716	10.5	.4134	29	1.1417	63	2.4803	94	3.7008
0.45	.0177	1.95	.0768	3.8	.1496	7	.2756	10.8	.4252	30	1.1811	64	2.5197	95	3.7402
0.5	.0197	2	.0787	3.9	.1535	7.1	.2795	11	.4331	31	1.2205	65	2.5591	96	3.7795
0.55	.0217	2.05	.0807	4	.1575	7.2	.2835	11.5	.4528	32	1.2598	66	2.5984	97	3.8189
0.6	.0236	2.1	.0827	4.1	.1614	7.3	.2874	12	.4724	33	1.2992	67	2.6378	98	3.8583
0.65	.0256	2.12	.0835	4.2	.1654	7.4	.2913	12.5	.4921	34	1.3386	68	2.6772	99	3.8976
0.7	.0276	2.15	.0846	4.25	.1674	7.5	.2953	13	.5118	35	1.3780	69	2.7165	100	3.9370
0.75	.0295	2.2	.0866	4.3	.1693	7.6	.2992	13.5	.5315	36	1.4173				
0.8	.0315	2.24	.0882	4.4	.1732	7.7	.3031	14	.5512	37	1.4567				
0.85	.0335	2.25	.0886	4.5	.1772	7.8	.3071	14.5	.5709	38	1.4961				

MOVE THE DECIMAL POINT IN EACH COLUMN FOR LARGER OR SMALLER MULTIPLES OF DIMENSIONS